A Study of Low-Power Ultra Wideband Radio Transceiver Architectures

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Abstract - **This paper studies low-power ultra wideband (UWB) transceiver architectures. First, three different architectures for the impulse-radio UWB transceiver are studied, while investigating the power-performance tradeoffs. The paper illustrates that a more power-efficient architecture should perform part of the signal processing in the analog-domain. Next, the multiband UWB transceiver is studied and power-efficient circuits for the front-end of the UWB transceiver are presented. Finally, the performance and power consumption of these transceivers are compared and a number of design indications are provided.**

I. Introduction

UWB wireless radios are capable of carrying extremely high data rates for up to 250 feet with little transmit power. Furthermore, the spread spectrum characteristics of UWB wireless systems, and the ability of the UWB wireless receivers to resolve the multipath fading due to the nature of the wireless impulse transmission, make UWB systems a promising wireless for a variety of high-rate, short- to medium-range wireless communications. UWB technology is at present defined by the FCC as any wireless transmission scheme that occupies a fractional bandwidth (BW/$f_c \geq$ 20% (where BW is the transmission bandwidth and f_c is the band center frequency), or more than 500 MHz of absolute bandwidth. Furthermore, it must meet the spectrum mask specified by the FCC, and shown in Fig. 1 [FCC02], [Roy04]. This 7.5GHz of unlicensed bandwidth has attracted the consumer electronics and automobile manufacturers to think of some exotic applications, such as information station concept, and wireless DVD quality audio/video transmission. Moreover, the UWB definition has given system designers the opportunity to employ two approaches to UWB system design: (1) single-band impulse radio [Win98], [Win00], and [Mireles01], and (2) multiband radio [Somayazulu02], [IEEE802.15.3a], [Stroh03], and [Aiello03]. The signal bandwidth in UWB impulse radio systems can spread over the whole 7.5GHz of allowable bandwidth, and therefore, similar to any other spread-spectrum system, UWB impulse radio is less susceptible to any narrowband frequency interference. Furthermore, the relative simplicity of this implementation compared to the super-heterodyne architecture manifests itself to a lower power consumption for impulse-radio UWB architectures

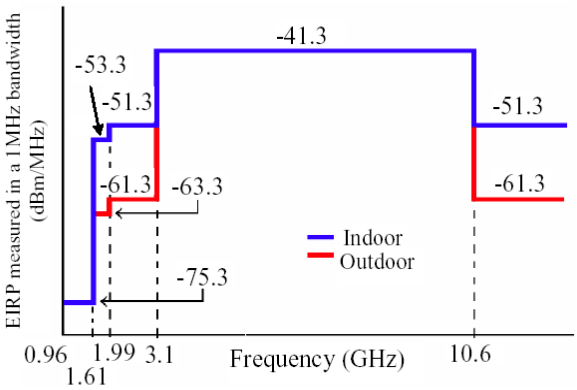

Fig. 1. UWB spectral mask and FCC Part 15 limits.

On the other hand, the new definition of UWB has averted the viewpoint of the UWB community from impulse radio to well understood schemes such as multiband CDMA and OFDM. In a multiband system, UWB coexistence with IEEE 802.11a (5GHz carrier frequency) is improved through adaptive band selection [Batra03]. In contrast to impulse-radio, pulse generation is not an issue in a multiband architecture.

The goal of this paper is to provide a study of various low-power architectures for the UWB wireless radio and to identify existing tradeoffs among these transceiver architectures. The study includes both the impulse-radio as well as the multiband wireless transceivers. Various circuit/system design techniques are examined to reduce power consumption.

The remainder of the paper is organized as follows: Section II summarizes the basic characteristics of the UWB wireless communications. Section III studies the power consumption of various impulse-radio architectures. Section IV describes the design challenges for the design of the power-hungry RF frond-end of the multiband UWB transceiver. Finally, Section V provides the concluding remarks.

II. Basic Characteristics of The UWB Radio

From a communications theory perspective, perhaps the most important characteristic of UWB systems is their capability to operate in the power-limited regime. This attribute is comprehended using Shannon's equation for the channel capacity [Shannon48], [Proakis01]:

$$C = B\log\left(1+\frac{BS_0}{BN_0}\right) \quad \text{bit/sec} \qquad (1)$$

where C is the channel capacity, B is the bandwidth in Hz, S_0 is the signal power spectral density (PSD) in W/Hz and $N_0/2$ is the noise single-sided PSD in W/Hz [Proakis01]. For a UWB wireless network, the bandwidth will likely be much higher than the data rate, so that the system can operate at very low signal to noise ratios (SNR). This means that a UWB wireless network is able to achieve high data rates with relatively low transmit power. A key point is that in the power-limited regime, the capacity increases almost linearly with power, whereas in the bandwidth-limited (high SNR) regime, capacity increases only as the logarithm of signal power (which means that a linear increase in data rate requires exponentially more power). This fact also highlights the importance of a power efficient modulation format in the design of a UWB system, i.e., a small disadvantage in power efficiency directly translates to a corresponding reduction in throughput [Welborn01]. Table 1 summarizes the comparison between the UWB radio and the conventional narrowband systems (e.g., 802.11a/b/g).

Table 1: Comparison between narrowband and UWB communication systems

UWB radio	Narrowband wireless
Low transmit power	High selectivity
Low immunity to noise/interference	High immunity to noise/interference
high data rate	Low data rate
WPAN	WLAN, WMAN

III. Low-Power Impulse-Radio UWB Transceivers

In general, the impulse-radio UWB directly modulates an impulse-like waveform with sharp rise/fall times, which occupies

several GHz of bandwidth. In earlier work, a typical *baseband* UWB pulse, also called monopulse, such as the Gaussian monopulse obtained by differentiation of the standard Gaussian waveform has been used frequently for analytical evaluation of UWB systems [Win98], [Win00]. One such wideband pulse that is better suited to spectral control within the mask is [Roy04]:

$$p_h(t) = W(t)\cos(2\pi f_c t) \quad (2)$$

The signal $p_h(t)$ is generated by a window signal $W(t)$, which is modulated by a carrier frequency f_c. The window signal can be any commonly used window function, such as Hamming, Hanning, or Bartlett window functions. The pulse $p_h(t)$ is characterized by two parameters f_c and f_s, where f_c is the desired center-of-band frequency, and f_s is a modulation frequency that primarily impacts the bandwidth of the transmitted signal.

Depicted in Fig. 2 is a prototypical impulse-radio UWB transceiver. This transceiver can be used for the same applications targeted for use with Bluetooth, but at higher data rates and lower emitted radio frequency (RF) power. The information is modulated using several different techniques: the pulse amplitude could be modulated with ± 1 variations (bipolar signaling) or $\pm M$ variations (M-ary pulse amplitude modulation or MPAM), turning the pulse on and off (known as on/off keying or OOK), or dithering the pulse position (known as pulse position modulation or PPM). The pulse has a duration on the order of 200ps and, in this example, its shape is designed to concentrate energy over the 3.1-10.6GHz bandwidth. An important attribute of the impulse-radio transmitter is that the power amplifier may not be required in this case because the pulse generator needs only produce a voltage swing on the order of 100mV. As with the superheterodyne radio, a bandpass filter (BPF) with a 7.5GHz bandwidth is used before the antenna to constrain the emissions within the desired frequency band.

In an impulse-radio UWB receiver, the analog-to-digital converter (ADC) can be moved almost up to the antenna after the low-noise amplifier (LNA) and variable-gain amplifier (VGA), as also shown in Fig. 2, thereby performing much of the signal processing in digital domain. Critical to this design approach, however, is the ability of the ADC to efficiently sample and digitize the received signal at least at the signal Nyquist rate of several gigahertz.

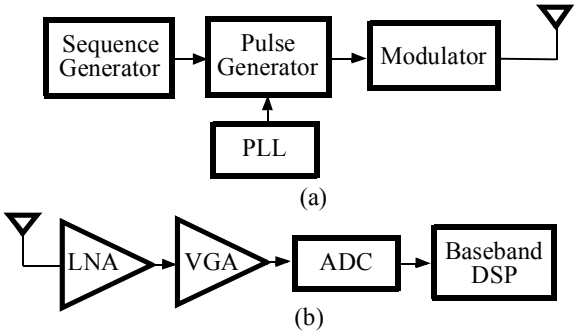

Fig. 2. The building block of an impulse-radio transceiver, (a) transmitter, and (b) receiver.

For instance, for a single-band signal using the 7.5GHz available FCC band, the constituent ADC must have a sampling-rate of at least 15 Gsamples/sec, which is an excessively high sampling rate! A relatively simple temporal variation of each monopulse in the single-band scheme allows us to employ low-resolution ADCs (e.g., 4-6 bits). Furthermore, the ADC must also support a very large dynamic range to resolve the received signal from the strong narrowband interferers. A low resolution, multi-gigahertz conversion rate suggests the use of full-flash data converters [Razavi95].

An underlying advantage of the UWB radio lies on its low-power consumption requirement. The constituent ADC is the bottleneck for the performance and power consumption of the receiver in Fig. 2 (b). The most power-hungry subsystem in a full flash N-bit ADC is the comparator bank comprising 2^N-1 comparators. Using the simple formula $P_{avg} = 2^{N-2}(\gamma^{-1}C_S V_{ref}^2 f + (1-\gamma)^{-1} V_{DD} I_{DD})$ (where N is the resolution, C_S is the equivalent switched capacitance of each comparator, V_{ref} is the reference voltage for the ADC conversion, f is the clock frequency of the comparator, γ is the fraction of the clock period used for comparison, V_{DD} is the supply voltage, and I_{DD} is the DC current drawn from the supply voltage) as a crude approximation for the power consumption of the comparator bank, a 4-bit 15GHz flash ADC can easily consume hundreds of milliwatts of power. The comparators must be able to detect the voltages around or below half LSB [1-LSB (in volts) = $V_{ref}/2^N$] within a given time interval determined by the clock signal. However, designing a clock comparator at a clock frequency of 15GHz is beyond the frequency capabilities of the current subquarter micron CMOS technology. This is because such high-speed comparator needs to have a preamplifier stage with a unity gain-bandwidth of 330GHz [$\approx 2.2/(0.1T_{clk})$, assuming the rise- and fall-times of the clock signal are 10% of the clock period, T_{clk}]!

Recently, [Hoyos04] presented an algorithmic approach for the high-speed ADC of the UWB signals based on the quantization of the coefficients obtained by the projection of a continuous-time signal over an orthogonal space. This approach exploits the signal representation in domains other than the classical time domain, leading to reduced speed at the comparators that perform the quantization of the sampled signal, and potentially improves the distortion versus average bit rates of the ADC [Hoyos04]. However, a major challenge lies in the silicon implementation of this approach.

The above obstacles can be alleviated to some extent using three different approaches: (1) time-interleaved architectures, (2) frequency-domain channelizing, and (3) signal processing in the analog-domain. These approaches will be illustrated in the following sections.

A. Time-Interleaved Architectures

To relax speed as well as power consumption requirements of the constituent ADC, the data conversion can be combined with the decimation of sampling frequency. To retain the conversion rate, the sampling decimation must however be undertaken using a parallel number of time-interleaved data converters. Fig. 3 shows the receiver block diagram of the system that employs decimation and time-interleaving.

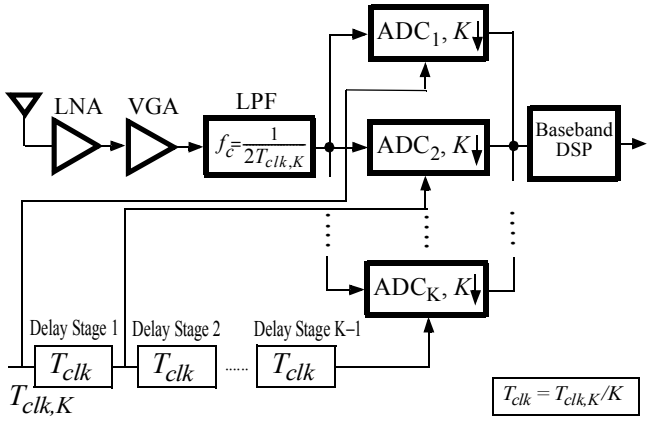

Fig. 3. Receiver block diagram of the time-interleaved architecture.

Each ADC in the time-interleaved architecture performs at a sampling period which is an integer multiple of the original sampling rate. Clock signals to the ADCs are provided by a delay chain, as shown in Fig. 3. The ADCs controlled by equally delayed clock signals thus operate as a full-rate ADC. Despite relaxing the sampling rate of the data converter, the time-interleaved architecture still receives the same UWB signal, which causes the aliasing. An anti-aliasing filter with a cutoff frequency of $f_c = 1/(2T_{clk,K})$ is thus needed, as shown in Fig. 3. The power consumption of the system in Fig. 3 is still comparable to that of Fig. 2, because the K ADCs in

Fig. 3 operate simultaneously at a sampling rate which is $1/K^{th}$ of the ADC in Fig. 2.

B. Frequency-Domain Channelization

As another approach to relax the ADC stringent requirements, channelization can be achieved using a bank of mixers operating at equally spaced frequencies within the 3.1-10.6 GHz band, and low-pass filters to decompose the analog input signal into subbands [Namgoong03]. Frequency-domain channelization of the received signal using this approach greatly relaxes the design requirements of the ADCs, making it possible for the ADC to incorporate a front-end sample-and-hold (S/H) circuit. Although the full-flash ADCs incorporating clocked comparators do not need to employ a separate S/H circuit, they will also benefit from this technique. This is because each ADC sees only the bandwidth of the channelized subband, which is a fraction of the whole signal bandwidth; as opposed to the time-interleaved architectures. The system block diagram of a frequency-domain channelized UWB receiver is depicted in Fig. 4. The system first downconverts the signal to various lower frequencies using $K-1$ analog mixers. The LO frequencies are chosen appropriately such that all subsequent frequency channels are downconverted to the same lower-frequency subband. The down-converted signals are then passed through bandpass filters with the same lower corner frequency of 3.1GHz and the upper corner frequency of $f_c = f_{clk,K}/2$. The constituent ADCs used to digitize the downconverted subbands will thus be identical with a sampling frequency of $f_{clk,K}$. Finally, the original digitized subbands are reconstructed using the frequency upconversion in the digital domain.

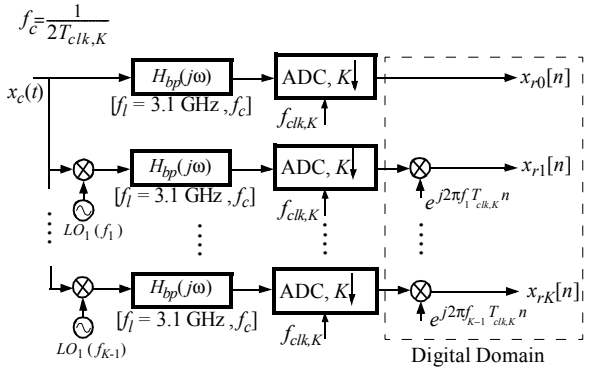

Fig. 4. Receiver block diagram of the frequency channelized UWB receiver.

The system in Fig. 4 alleviates some of the major drawbacks of time-interleaved architectures. First of all, the input signal to each ADC is band-limited. Therefore, there is no need to filter out the valuable high-frequency content of the signal. Furthermore, each ADC in Fig. 3 sees the UWB received signal, making it almost impossible to design flash ADCs with separate front-end S/H circuits in standard CMOS process. On the other hand, the ADCs in Fig. 4 need satisfy relaxed high-frequency requirements, as the input signals to the ADCs are now channelized to a much narrower frequency band from 3.1–f_c GHz.

The frequency-channelized UWB receiver, however, consumes more power compared to the time-interleaved receiver. The bandpass filters must have a sharp roll-off with a large attenuation in the stop-band, which necessitates a high-order filter design. For instance, designing a Butterworth filter with cutoff frequencies $f_l = 3.1\text{GHz}$, $f_c = 4.6\text{GHz}$, 50-Ω input and load terminations, a 50-Ω characteristic impedance, and the stop-band attenuation of 50dB leads to a 4th-order LC filter shown in Fig. 5 (a) [Chen86]. Fig. 5 (b) demonstrates the frequency response of the BPF of Fig. 5 (a).

The constituent BPFs consume large die area because of large inductors used in the BPFs, some of those must be realized using off-chip components. Of particular concern is the fact that the frequency channelized system must employ $K-1$ mixers and local oscillators (LO), which contribute to an increase in average power dissipation.

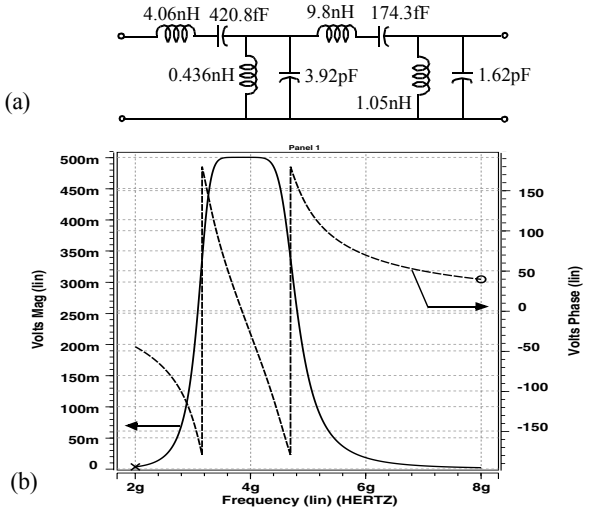

Fig. 5. (a) the circuit schematic of a passive 4th-order Butterworth BPF, and (b) the frequency response of the BPF.

The foregoing discussion reveals that the design of data converters for the UWB radio transceivers will be challenging. In addition, the data converters are power hungry devices, and techniques used to relax some of the challenges for the converter design do not necessarily contribute to the reduction of power consumption.

C. More Signal Processing in the Analog-Domain

The digital signal processing alleviates some of the design challenges encountered in the analog domain. As mentioned above, the impulse-radio UWB allows the transfer of the ADC close to the antenna (after LNA), thereby making it possible to do the signal recovery and demodulation in digital domain. However, this may not provide a low-power solution.

One possible solution to reduce power consumption is to move the ADC down and place it next to the time-domain correlator, and perform the down-conversion or the time-domain correlation subsystem using analog technique. Shown in Fig. 6 is the system block diagram of the UWB impulse-radio transceiver incorporating a time-domain RF correlator.

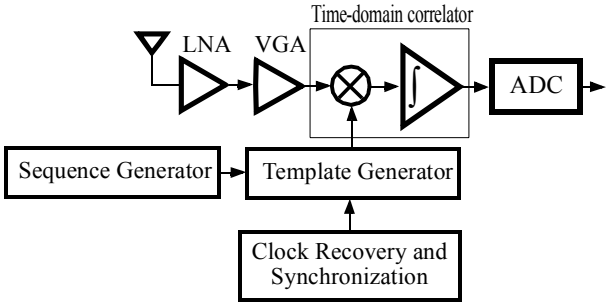

Fig. 6. The block diagram of the impulse-radio UWB wireless receiver with time-domain correlator being realized in analog-domain.

Similar to Fig. 1, the synchronized short duration pulses are modulated, and then sent to the antenna. At the receiver, the energy collected by the antenna is amplified using a UWB LNA and passed through a time-domain correlator. For a transmitted Gaussian monopulse, the ideal template in the receiver should naturally employ a Gaussian signal. Nevertheless, generating this Gaussian template is difficult and power-consuming. Since the received signal of the UWB receiver can be appropriately fitted using a sinusoidal wave, a power-efficient design solution is to employ a frequency

synthesizer, synthesizing sinusoidal waves. An example of time-domain correlation using the sinusoidal template is shown in Fig. 7.

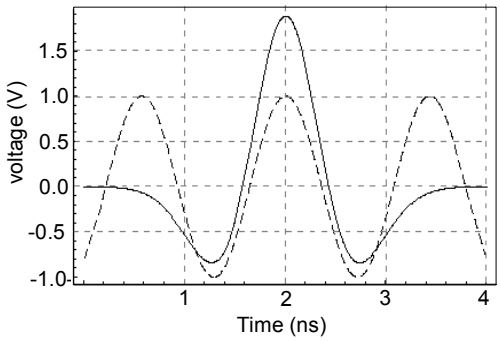

Fig. 7. time-domain correlation using a sinusoidal template.

Clearly, a major concern is to be able to design a low-power transceiver including LNA/mixer, clock recovery, and template generator. In general, designing the RF front-end sub-system of any UWB transceiver poses a great challenge for the implementation of the whole transceiver due to the stringent requirement of the UWB radio. For instance, the LNA and mixer in the receive path must operate across the whole system's frequency spectrum, that is, from 3.1GHz to 10.6GHz. The template generator must generate high-frequency signals while providing immunity to temperature and process variations [IEEE802.15.3a].

The conventional design techniques, such as inductive degeneration, and matching for the optimum power gain and noise figure are valid only for narrowband signals around a center frequency, hence, inappropriate for the UWB applications. To achieve multi-gigahertz bandwidths, new circuit topologies for the LNA/mixer, power amplifier, and frequency synthesizer need to be explored. The receiver system of Fig. 6, however, relaxes the design requirements of the constituent ADC.

Example: A UWB Distributed CMOS Mixer

In an attempt to design an ultra wideband mixer, we designed and fabricated a novel distributed CMOS mixer in a 0.18µm CMOS process [Safarian05]. Each mixer cell within the distributed proposed architecture constitutes a lumped active mixer, such as single-balanced or double-balanced circuit. Each cell is realized using a fully differential single-balanced circuit. The IF component at the output of each constituent cell is obtained by mixing the input RF voltage with the LO signal. To compromise between the area and circuit performance (including the 3rd intercept point (IIP3), the flatness of the conversion gain over the bandwidth, and noise figure (NF)), a 2-stage distributed mixer was designed and fabricated. Shown in Fig. 8 is the circuit schematic of the mixer circuit. Fig. 9 indicates the die photo of the actual fabricated UWB mixer.

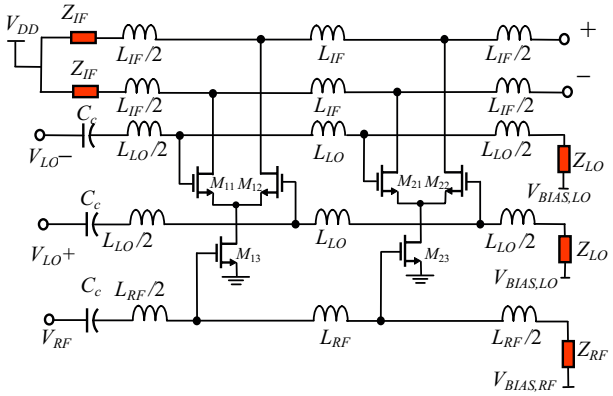

Fig. 8. The circuit schematic of a 2-stage UWB mixer.

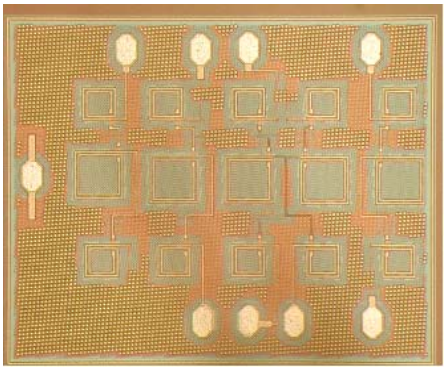

Fig. 9. The die photo of the circuit of Fig. 8.

The die is mounted on a 4 metal-layer high-frequency board, and directly wire-bonded. The micro-strip lines directly connect the wire-bonded pads to the connectors. A 1.8-V supply voltage is used in the design. The overall power consumption of the mixer is 10.4mW [Safarian05].

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The template generator and the clock recovery are combined and realized using a PLL-based frequency synthesizer. An example of a low-power frequency synthesizer is a 5GHz synthesizer proposed in [Pellerano04], which consumes a total power consumption of 13.5mW. This PLL shows the capability of CMOS technology for the high-frequency low-power synthesizer design. Table 2 provides the performance summary of some frequency synthesizers operating around the frequency range of UWB radio.

The output signal of the integrator is a lower-frequency signal representing the correlation between the template and the received signal. The presence of the clock recovery also helps localize the received monopulse, and as a consequence, filter out the high-frequency component of the mixer output. The required sampling-rate of the ADC is thus reduced considerably.

Table 2: A performance summary of various state-of-the-art frequency synthesizers

Ref.	Technology	Frequency	Power	Phase-noise (1MHz offset)
[Pellerano04]	0.25µm CMOS	5GHz	13.5mW	-116dBc/Hz
[Tiebout04]	0.13µm CMOS	13GHz	60mW	-102.34dBc/Hz
[Herzel03]	0.25µm BiCMOS	4.72GHz	58.75mW	not reported
[Zargari02]	0.25µm CMOS	5.34GHz	180mW	-112dBc/MHz

IV. Low-Power Multiband UWB Transceivers

So far, the effort has been mainly focused on the impulse radio, that is, using extremely short pulses to transmit information. Short pulses have very large bandwidth and their duty cycle can be very small allowing very low power transmitters without requiring carrier modulation. The underlying problem of impulse radio lies in the difficulty of the enabling technology to generate, send, and receive extremely short pulses with sub-nanosecond duration.

In a multiband UWB transceiver, the whole 3.1-10.6GHz bandwidth is split into 528MHz subbands, as illustrated in Fig. 10. Time-frequency codes are utilized to interleave data sequences in different bands, thereby achieving spread-spectrum communications. Either single-carrier or multi-carrier modulation may be employed in each subband. Single-carrier modulation facilitates the design of inexpensive transmitters, however, at the cost of more complicated receivers. Multi-carrier modulation, also known as OFDM, widely used in the

implementation of IEEE 802.11.a/g, HIPERLAN II, DVB, DAB standards and xDSL technology, performs well in dispersive channels, and enables high rate communication with inexpensive low-power receivers. When combined with guard interval and cyclic prefix, OFDM eliminates ISI/ICI, and overcomes fading by using forward error correction (FEC) coding [Bingham90].

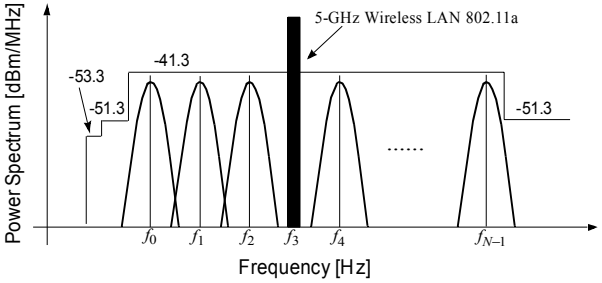

Fig. 10. The bandplan for the UWB multiband OFDM. The fourth band is null to filter out the strong 802.11a interference.

The channel estimate can be incorporated into a soft decision Viterbi decoder in a bit-interleaved coded modulation (BICM) fashion to get more coding gain, and have the system operate in lower SNRs. In a multiband OFDM system, OFDM symbols are interleaved along different frequency bands, hence yielding frequency diversity as well. Another advantage of OFDM is its capability to capture multi-path energy with a simple fast Fourier transform (FFT), in contrast to CDMA and impulse radio, where rake correlator fingers should be used to exploit multi-path diversity. The rake correlators in CDMA-based UWB receivers lead to a more complex receiver with a higher power consumption. OFDM enables us to adapt our system to avoid using some specific bands to comply with other regulations set forth by other countries. This is easily achieved by modulating "null" on some sub-carriers eliminating the need for narrowband notch filters. Problems with OFDM are the complexity of the transmitter, and high peak-to-average power ratio (PAPR) of OFDM signal causing distortion in power amplifier used in the transmitter. Considering all the pros and cons, a multiband OFDM results in a highly satisfactory trade-off between different design criteria and a low-power multiband UWB transceiver. Figs. 11 (a) and (b) show the transmitter and receiver systems of the multiband OFDM UWB transmitter and receiver, respectively.

Similar to a conventional OFDM system, the UWB system employs (1) a scrambler to make data look random eliminating long runs of ones and zeros as well as repetitive patterns, (2) an interleaver to spread burst errors in time, (3) a quadrature amplitude modulation (QAM) mapper to achieve higher bit-per-symbol, and (4) a convolutional encoder to realize the error correction coding scheme.

An important concern regarding the multiband OFDM UWB transceiver is its need of an RF power amplifier in the transmitter. The impulse-radio counterpart does not require the RF power amplifier, because the pulse generator needs only produce a short pulse with hundreds of millivolts of amplitude. CMOS distributed amplifiers proposed in [Ahn02] and [Yazdi05] can be used as class-A power amplifiers for the multiband UWB transceiver. However, the power consumption of distributed power amplifiers are considerably large. For instance, [Ahn02] reports a power dissipation of 216mW from a 3.0V supply voltage.

The multiband approach accommodates baseband processing over smaller bandwidths, thereby relaxing the design constraints on the key components of the UWB transceiver, most notably the data conversion modules. Conventional circuit techniques can be employed to implement the data conversion circuits [Choi01]. More precisely, the ADC is now digitizing the 528MHz downconverted signal. Designing a power-efficient flash ADC with a sampling rate of 1.1 Gsamples/sec is quite achievable in standard CMOS process [Choi01].

In spite of simplifying the ADC design, the front-end LNA/mixer still entails design challenges similar to the impulse-radio system, for instance, (1) a minimum gain of 6dB, (2) a maximum NF of 10dB, and (3) a minimum third-order intercept point (IIP3) of -5dBm. Notice that these requirements must be satisfied over the 7.5GHz bandwidth set forth by the FCC for the UWB communications, which makes the design of the UWB LNA/mixer even more challenging.

The first circuit solution is to incorporate a bank of LNA/mixers, each associated with a subband. However, this circuit solution suffers from two important drawbacks: (1) The band switching at UWB frequency range should be realized using low-loss high-frequency switches making the use of MOS devices inappropriate. (2) The power consumption of the circuit will be close to 1W.

The second solution is to design single a LNA/mixer circuit for the entire 3.1-10.6 GHz frequency band. The band selection is thus achieved by means of the multiband frequency synthesizer. This circuit solution is much more power efficient than the former one. As an example, the mixer circuit of Fig. 8 can be incorporated in a multiband UWB receiver.

The frequency synthesizer employed in both transmitter and receiver units in Figs. 11 (a) and (b) should synthesize low-jitter center frequencies of all subbands in Fig. 10. In addition, a major constraint incurred in the design of such frequency synthesizer lies in its capability to achieve multi-nanosecond hopping time between the subbands. This notion demands concurrent synthesis of all center frequencies and selection of the appropriate center frequency using a multiplexer that is controlled by an external select signal from baseband processor.

Table 3 summarizes the power consumption of the various building blocks of the RF front-end for the time-interleaved UWB receiver, the frequency channelized UWB receiver, the impulse radio receiver incorporating analog time-domain correlator, and multiband UWB receiver. The comparison is made for the receiver architectures, because the transmitter in the multiband ODFDM clearly consumes more power than the one in the impulse-radio. Moreover, all the impulse radio systems use the same transmitter architecture.

As indicated in Table 3, the frequency synthesizer in the multiband OFDM receiver approximately consumes 11dB [$=10\log(P_{MB}/P_{IMPULSE})$] more power than the impulse-radio systems. This is because the frequency synthesizer must synthesize low-jitter center frequencies for all constituent subbands concurrently [IEEE802.15.3a].

V. CONCLUSIONS

This paper studied low-power ultra wideband (UWB) transceivers. Three different architectures for the impulse-radio UWB transceiver were studied, while investigating the power-performance tradeoffs. it was shown that a more power-efficient architecture should carry out part of the signal processing in the analog domain. Furthermore, the multiband UWB transceiver was studied and power-efficient circuits for the front-end of the UWB transceiver were presented.

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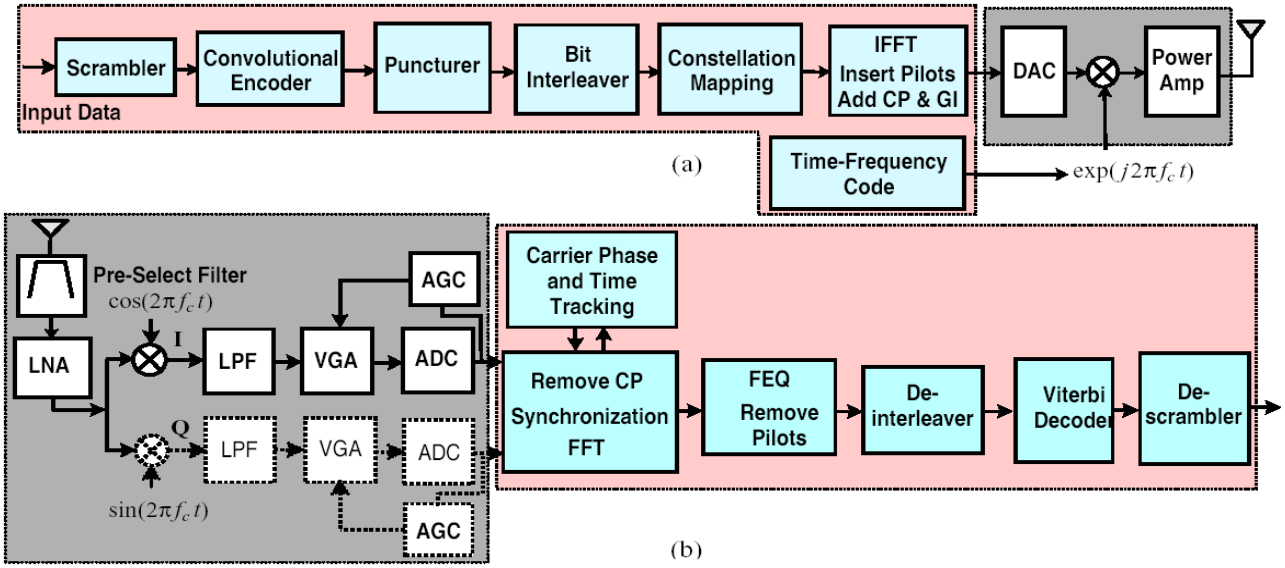

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Table 3: Performance and power consumption comparisons of three different UWB receiver architectures

	LNA Reference, Power	Mixer Power	Frequency Synthesizer Reference, Power	ADC		Overall
				Sampling rate, Power	Resolution	
Time-interleaved, decimating factor: 4	[Bevilacqua04], 9mW	–	[Pellerano04], 13.5mW	3.75Gsamples/sec, 180mW (45x4)	4	202.5mW
Frequency channelized, 4 channels	[Bevilacqua04], 9mW	–	[Pellerano04], 13.5mW	3.75Gsamples/sec, 220mW (55x4)	4	242.5mW
Impulse-radio with analog correlator	[Bevilacqua04], 9mW	10.4mW	[Pellerano04], 13.5mW	3Gsamples/sec, 55mW	4	87.9mW
Multiband OFDM	[Bevilacqua04], 9mW	10.4mW	Multiband, 160mW	1.1Gsamples/sec, 25mW	4	204.4mW