Project 2. An 8-bit 4-Msamples/sec CMOS Nyquist-rate A/D Converter

Project description

In this project an 8-bit 5Msamples/sec CMOS Nyquist-rate A/D converter in 0.35 \( \mu \)m double-poly four metal CMOS technology will be designed. Although any type of Nyquist-rate A/D converter is allowed, the power consumption should be less than 60mW at full-speed of operation. The integral nonlinearity (INL) should be between 0.4-0.5 LSB. The differential nonlinearity (DNL) should be between 0.4-0.5 LSB. The SNDR at 2MHz is greater than 50dB.

To have a unique and comparable results please use the following MOS SPICE parameters that has been provided by MOSIS.

http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/tsmc-035/t14a_2p4m-params.txt

Cadence and HSPICE are both accepted for the reporting simulation results.

The final report should include:

1. A detailed description of the circuit building blocks
2. The detailed circuit schematics of each A/D block
3. The simulation results including
   3.1. The INL
   3.2. The DNL
   3.3. SNDR vs. input frequency

In the final presentation, each group should also demonstrate their HSPICE and Cadence simulations.

Students will do this project in small groups of two to three people.