A 10MHz-1GHz CMOS PLL in 0.18u Technology

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Design Goals

- Lock Range : 10Mhz – 1GHz
- Supply noise insensitivity.
- Phase noise < -60 dBc/Hz for a 200mV RMS supply noise at 10KHz for PLL operating at 800MHz.
- Power Consumption <40mW.
- Loop Phase Margin better than 60.
Block Diagram of a PLL

Phase Comparator

XOR Gate
Implementation of Phase Frequency Comparator

OUTPUTS OF PHASE FREQUENCY DETECTOR

- Case1. Same Phase and frequency
OUTPUTS OF PHASE FREQUENCY DETECTOR

- Case 2. Clock Lags VCO Output

OUTPUTS OF PHASE FREQUENCY DETECTOR

- Case 3. Clock Leads VCO Output
CHARGE PUMP

- What is a charge pump?

CHARGE PUMP IMPLEMENTATION
CHARGE PUMP SIMULATION RESULTS

LOW PASS FILTER
LOW PASS FILTER WITH AND WITHOUT C2

OSCILLATOR

- Oscillator is like a badly designed Feedback Amplifier
- For an amplifier under Feedback to oscillate at $\omega_0$, it should satisfy the following two criteria:
  - $|H(j\omega_0)| > 1$
  - Phase $H(j\omega_0) = 180^0$
HOW TO CONTROL THE FREQUENCY

- Cascade three Differential Amplifiers with sufficient gain
- The Delay time constant of each buffer is Output Resistance*Load Capacitance
- IDEA: Resistance of a MOS in linear region can be controlled by its gate to source voltage.

POSSIBLE IMPLEMENTATION

- The load of each buffer be replaced by a PMOS transistor in linear region
- By varying the Vgs of PMOS load, vary the output resistance.
  - $T_d = R \times C$
  - $T_d = K \times C/(V_{gs} - V_t)$
  - Frequency = $1/(2N \times T_d)$ controlled by varying $V_{gs}$
Problems with Implementation

- Extremely sensitive to supply voltage variations (supply noise).
- Output voltage swing varies considerably over the frequency range.
- Thus limited tuning range.

SYMMETRIC LOAD BUFFERS

- Symmetric loads have the following VI characteristics
How does such a characteristics help?

- The output voltages of buffers are symmetric about center of their swings. 
  \((\text{Vdd-Vcontrol})/2\)
- In presence of supply noise, there are equal and opposite charging currents in each branch and the net bias current remains constant.
- Change in Incremental Resistance almost zero.
- Delay \(\alpha\) Incremental Resistance.

Buffer with Symmetric load

![Buffer with Symmetric load diagram]
AC RESPONSE OF CASCADED BUFFER STAGES WITH SYMMETRIC LOAD

SELF BIASING SCHEME
What does self biasing achieve?

- The output voltage is bounded between Vdd and Vcontrol.
- Bias of the NMOS current transistor is varied to maintain the Voltage at drain of symmetric load at Vcontrol.
- Output current of the NMOS current source is established by the load element and is independent of the supply voltage.

DC characteristics of the Self Biasing Circuit - Sweeping V(control)
DC characteristics of the Self Biasing Circuit - Sweeping Vdd

Ring Oscillator Output – Sweeping V(control)
How to get VCO outputs rail to rail?

VCO outputs for different V(control)
Connecting the Blocks:
PLL operation at 100MHz

PLL operation at 1GHz (Before Locking)
PLL operation at 1GHz (After Locking)

PLL operation at 10MHz (Before Locking)
PLL operation at 10MHz (After Locking)

Modelling Supply Noise
PLL operation under 50mV supply noise (rms) at 800MHz

Phase noise measurement at 800MHz = -60dBc/Hz @100MHz offset
## Summary of Results

<table>
<thead>
<tr>
<th>SPECIFICATION</th>
<th>RESULT</th>
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</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.8v</td>
</tr>
<tr>
<td>Frequency of operation</td>
<td>10M-1G</td>
</tr>
<tr>
<td>The power consumption at 1.8V</td>
<td>40mw</td>
</tr>
<tr>
<td>(Average)</td>
<td>0.8mw</td>
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<tr>
<td>(Peak)</td>
<td>1.3mw</td>
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<tr>
<td>Phase noise at a frequency of 800MHz</td>
<td>-60dBc/Hz</td>
</tr>
<tr>
<td>With 200mV supply noise at 100MHz</td>
<td>-60dBc/Hz</td>
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<tr>
<td>frequency offset.</td>
<td></td>
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<td>Lock Acquisition Time</td>
<td>2us</td>
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## References

THANK YOU