A Comprehensive Study of Energy Dissipation in Lossy Transmission Lines Driven by CMOS Inverters

Payam Heydari
Department of Electrical and Computer Engineering
University of California
Irvine, CA 92697

Soroush Abbaspour and Massoud Pedram
Department of Electrical Engineering-Systems
University of Southern California
Los Angeles, CA 90089

Abstract - *In this paper, new formulations for the energy dissipation of lossy transmission lines driven by CMOS inverters are provided, and a new performance metric for the energy optimization under the delay constraint is proposed. The energy formulations are obtained by using approximated expressions for the driving-point impedance of lossy coupled transmission lines which itself is derived by solving Telegrapher's equations. A comprehensive analysis of energy is performed for a wide variety range of the gate aspect-ratios of the driving transistors. To accomplish this task, two stable circuits that are capable of modeling the transmission line for a broad range of frequencies are synthesized. Experimental results show that the energy calculated using these equivalent circuits are almost equal to the one calculated by solving the more complicated transmission line equations directly. Next, using a new performance metric the effect of geometrical variations of the interconnect and the driver on the energy optimization under the delay constraint is studied. The experimental results verify the accuracy of our models.*

1. INTRODUCTION

The semiconductor industry is continually moving toward the development and the implementation of smaller technology sizes. Recent studies on the effects caused by the nanometer technologies focus primarily on timing and signal integrity. However, only a handful of works have actually considered the deep sub-micron (DSM) effects on the energy dissipation of ULSI circuits [1][2]. The wiring system of a one-billion transistor die will deliver signal and power to each transistor on the chip, provide low-skew and low-jitter clock to latches, flip-flops and dynamic circuits, and also distribute data and control signals throughout the chip [3]. Providing the required global connectivity throughout the whole chip demands long on-chip wires that introduce large loading effects on the drivers. These global wires should deliver high frequency signals (presently at around 1.5-2.5GHz) to various circuits. This implies that global wires exhibit transmission line effects. So far, the well-known $(1/2)CV^2$ model has been used as an interconnect energy model, where C includes the capacitance of the interconnect and the capacitances of the both the driver and the driven circuits. V is the voltage swing. This model, however, fails to predict the interconnect energy dissipation in the current range of clock frequencies, where the signal transients do not usually settle to a steady state value due to the small clock periods. In paper [1], an analytical interconnect energy model with the consideration of event coupling has been proposed. Although this work addressed the effect of the capacitive coupling on the interconnect energy dissipation, it, however, used the distributed ladder RLC circuits to model the lossy transmission line effects.

In this paper, accurate expressions for the energy dissipation of interconnects driven by CMOS inverters are obtained. The dissipated energy is derived using approximated expressions for the driving-point impedance of lossy transmission lines. Furthermore a new performance metric is proposed that is relevant for the energy optimization under the delay constraint.

Section 2 presents two circuit model for the lossy transmission line; a new RLC circuit configuration called RLC-π circuit, and an RLC circuit. In section 3, the RLC-π and the RLC circuits are utilized to derive the total energy dissipation of a transmission line driven by a CMOS inverter for large W/L's and small W/L's of the driving transistors, respectively. Then a new metric is utilized that is very relevant for the energy optimization under the delay constraint. Simulations and experimental results provided throughout this section confirms the accuracy of our model and the usefulness of our metric. Finally, section 4 presents the conclusions of our paper.

2. LOWER-FREQUENCY MODELS FOR THE LOSSY TRANSMISSION LINE

At the current clock frequencies the propagation delay of signals traveling through the chip global wires is comparable to the time of flight. In other words, the line length is comparable to the propagated signal wavelength, λ, which is on the order of 0.6-2.1cm. This implies that transmission-line properties must be accounted for. It was shown in [4] that any two uniform parallel conductors, the signal and the current return path, that are used to transmit electromagnetic energy can be considered transmission lines. The current return path can be a ground plane, a ground conductor, or a mesh of ground lines on many layers. Solutions to Maxwell's equations for the electric and magnetic fields around conductors are current and voltage waves. The solution is completely determined in terms of the *characteristic impedance*, Z_o, and the *propagation constant*, γ. Consider a single lossy transmission line that is driven by a CMOS inverter, as shown in Fig. 1.

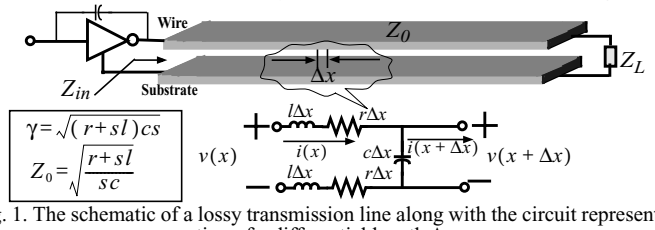


Fig. 1. The schematic of a lossy transmission line along with the circuit representation of a differential length Δx

The driving-point impedance of this transmission line is obtained using the voltage and current wave equations at the input port:

$$Z_{in}\big|_{x=-h}=\frac{V_i e^{\gamma h}+V_r e^{-\gamma h}}{I_i e^{\gamma h}-I_r e^{-\gamma h}}=Z_0\left(\frac{1+\Gamma_L e^{-2\gamma h}}{1-\Gamma_L e^{-2\gamma h}}\right)=Z_0\frac{Z_L+Z_0\tanh(\gamma h)}{Z_0+Z_L\tanh(\gamma h)} \quad (1)$$

where h is the line length. In the above equation, the load impedance, Z_L, is normally a capacitive load in ULSI circuits, since the interconnect normally drives a CMOS circuit whose input impedance is purely capacitive.

According to Eq. (1), the input impedance of a transmission line is a nonlinear function of frequency. Direct substitution of this nonlinear expression into the energy equation (which is the integral of the voltage-current product) does not yield a closed-form expression for the energy dissipation of the lossy transmission line. Still it is possible to simplify Eq. (1), using an observation, and obtain an accurate expression for the energy dissipation.

Observation 1. If the abrupt transitions of the input waveform are sufficiently far away in time so as to allow the circuit to come very close to its steady-state response, then the total energy delivered by the input source is obtained using the driving-point impedance of the circuit evaluated at low frequencies.

This observation is utilized here to simplify Eq. (1). We evaluate *tanh*(.) at low frequencies by expanding its Taylor expansion around $s = 0$ and truncating higher order terms. Depending upon the order of the truncation, two stable equivalent circuits are extracted.

A. First-order truncation

The first-order Taylor expansion of $\tanh(\gamma h)$ is γh. This leads to the following approximated rational function:

$$Z_{in}\big|_{x=-h}=\frac{1}{C_L s}\left[\frac{1+\left(\gamma^2 h^2\frac{C_L}{C_{int,tot}}\right)}{1+\frac{C_{int,tot}}{C_L}}\right]. \quad (2)$$

where $C_{int,tot}$ is the total interconnect capacitance including the Miller capacitance of the neighboring lines that are capacitively coupled to this line, and the interconnect-to-substrate capacitance. Using Eq. (2) a series RLC circuit is synthesized as also shown in Fig. 2.a, where R_{eq} and L_{eq} are defined as follows:

$$R_{eq}=\frac{C_L}{C_L+C_{int,tot}}R_{int}\ ,\ L_{eq}=\frac{C_L}{C_L+C_{int,tot}}L_{int,tot} \quad (3)$$

R_{int} is the line resistance. $L_{int,tot}$ is the total inductance of the lossy line including the self and mutual inductances. The inductive couplings between transmission lines are accounted for by an algebraic summation of

each line's self inductance and all mutual inductances between that line and other lines considering also the current direction flowing through the lines.

B. Second-order truncation

The second-order truncation of the Taylor series expansion of $\tanh(\gamma h)$ is:

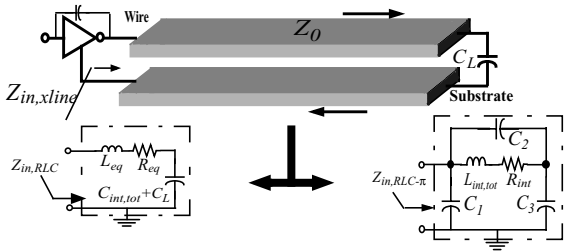
$$\tanh(\gamma h)=\frac{\sinh(\gamma h)}{\cosh(\gamma h)} \rightarrow \frac{2\gamma h}{2+\gamma^2 h^2} \quad , \ \textit{for smaller values of } |s| \tag{4}$$

This leads to the following relationship:

$$Z_{in}\big|_{x=-h} = \frac{1}{C_L s}\left[\frac{2+\gamma^2h^2+\left(2\gamma^2h^2\ \frac{C_L}{C_{int,tot}}\right)}{2+\gamma^2h^2\ +\left(2\ \frac{C_{int,tot}}{C_L}\right)}\right] \tag{5}$$

It would be instructive if one could propose a stable circuit realization whose impedance is expressed by Eq. (5). It is easily proven that for a lossy transmission line whose driving-point impedance at lower frequencies is expressed by Eq. (5), a new stable RLC-π equivalent circuit realization with an identical input impedance can be synthesized. The circuit structure is depicted in Fig. 2.b. C_1, C_2, and C_3 are related to the actual capacitances of the line and the load through the following relationships:

$$C_3=\sqrt{\frac{(C_{int,tot}+C_L)^2+C_L^2}{2}}\ ,\ C_2=\frac{C_{int,tot}}{2}+C_L-C_3\ ,\ C_1=C_{int,tot}+C_L-C_3 \tag{6}$$



(a) RLC equivalent circuit (b) RLC-π equivalent circuit

Fig. 2. A lossy transmission line and its equivalent circuit representations

Fig. 3 shows the magnitude response of the driving-point admittance of a lossy transmission line which is electromagnetically coupled to a similar line. The line electrical parameters are also indicated in Fig. 3. First, the circuit is simulated using star-HSPICE. Eq. (1) is then utilized and the magnitude response of the admittance function is calculated. As indicated in Fig. 3, the results obtained by HSPICE and by Eq. (1) are exactly the same and are indistinguishable from each other. In the next step, the magnitude response of the driving-point admittance of the equivalent RLC-π circuit is calculated. According to Fig. 3, this circuit accurately represents the driving-point admittance of a lossy coupled transmission line in lower frequencies up to 32GHz. Therefore according to Observation 1, the energy calculations using the RLC-π circuit yield expressions that are exactly equal to those of the actual coupled lossy line. Finally the magnitude response of the driving-point admittance of the equivalent RLC circuit is calculated and compared with those of RLC-π equivalent circuit and the lossy coupled line, as is also shown in Fig. 3. The RLC-π circuit models the lossy line more accurately than the RLC circuit in a broader range of frequencies.

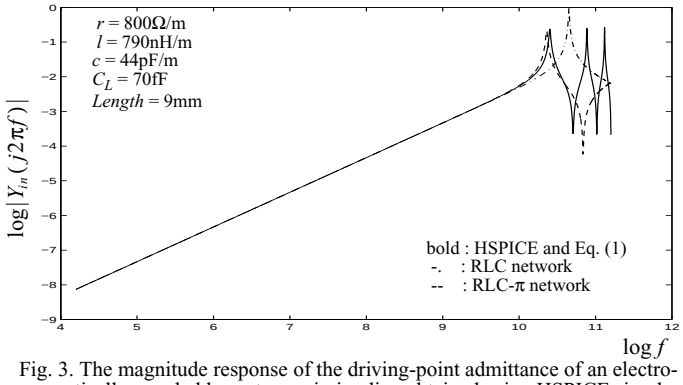


Fig. 3. The magnitude response of the driving-point admittance of an electromagnetically coupled lossy transmission line obtained using HSPICE simulation, using the direct simulation of Eq. (1), and by replacing the line with its equivalent RLC-π circuit, and with its equivalent RLC circuit

Both RLC-π and RLC equivalent circuits synthesized for a lossy coupled transmission line are utilized to compute the interconnect driving-point impedance and the interconnect energy dissipation. A lossy transmission line driven by a large driver is modeled by the RLC-π equivalent circuit, whereas the one driven by a small driver is modeled by the RLC circuit. Using equivalent RLC-π and RLC circuits, section 3 provides a comprehensive analysis of energy dissipation of the lossy transmission lines driven by CMOS inverters.

3. ENERGY DISSIPATION OF LOSSY TRANSMISSION LINES

Consider the circuit shown in Fig. 2. that is composed of an inverter driving a lossy transmission line. The load is another CMOS gate that is connected to the output port of this lossy transmission line. The electromagnetic coupling effects are treated the same way as discussed in section 2. To encompass a wide range of driver sizes in the energy analysis, two separate analyses are performed. For the large drivers the RLC-π circuit is used to model the lossy line (Section 3.1), whereas for the small drivers, the RLC model is utilized (Section 3.2). Fig. 4.a shows the variations of the drain-source resistance of a short-channel PMOS transistor in terms of its gate aspect-ratio. Comparing this variations with the magnitude response of a long lossy transmission line in Fig. 4.b sets forth the following criteria:

- If $r_{DS} \le \left(\frac{|V_{THp}|}{V_{DD}-|V_{THp}|}\right)|Z_{xline}|$, then the RLC-π circuit is used. (7)

- If $\left(\frac{|V_{THp}|}{V_{DD}-|V_{THp}|}\right)|Z_{xline}| < r_{DS} \le 2|Z_{xline}|$, then the RLC circuit is used. (8)

Please note that for $r_{DS} > 2|Z_{xline}|$, the inverter is incapable of driving the transmission line, and therefore the voltage swing is insufficient to maintain the correct circuit operation.

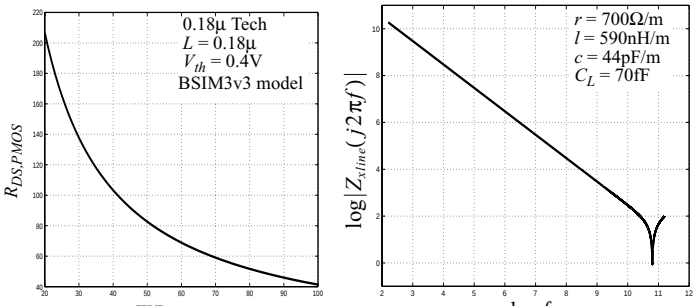


Fig. 4. (a) $r_{DS,PMOS}$ vs. the gate aspect-ratio (b) the magnitude response of the driving-point impedance of a lossy transmission line

Due to the changes in the operation regions of NMOS and PMOS transistors of the line driver during low-to-high and high-to-low transitions of the driver's output, we must distinguish between low-to-high and high-to-low transitions. During the low-to-high transition at the output, the PMOS transistor is conducting and provides a low-impedance conduction path from the supply to the load. During the high-to-low transition at the output the NMOS transistor is in "ON" condition, and no additional energy is transferred out of the power-supply.

We calculate the energy transferred out of the power-supply during a low-to-high transition. This energy is indeed the total dissipated energy per clock period of a CMOS gate that drives another CMOS circuit through a lossy coupled transmission line. The energy delivered by the power-supply through the gate in a low-to-high transition of the output is specified by Eq. (9).

$$E_{tot} = \int_{(L\rightarrow H)} V_{DD}\, i_{DD}(t)\,dt \tag{9}$$

where $i_{DD}(t)$ is the current flowing from the power-supply to the load and through the PMOS transistor during the low-to-high transition of the output.The energy dissipation E_{tot} is calculated for a step voltage at the driver input.

The current is obtained using the driving-point admittance of the circuit:

$$I_{DD}(s) = \frac{V_{DD}}{s}\, Y_i(s)$$

where $Y_i(s)$ is the driving-point admittance seen from the power-supply to the source connection of the PMOS transistor of the driver. $Y_i(s)$ consists of the admittance of the lossy line (that is modeled either using the RLC circuit or RLC-π circuit) and the PMOS device.

3.1. Energy calculation for lossy lines driven by large inverters

Consider a lossy transmission line that is driven by a large inverter. If the condition (7) is satisfied, then the lossy transmission line is modeled by the RLC-π circuit shown in Fig. 2.b whose electrical parameters are obtained

using Eq. (6). As for the inverter, it is known that the operating regions of the conducting transistors change during the input transition. This change of the operating regions makes the analysis cumbersome. On the other hand, for the fast input waveforms, the conducting transistors operate in the linear region for a large portion of the transition time [5]. As a result, we assume that the conducting transistor will be in the linear region for the entire input transition, and is modeled as an ideal switch along with the equivalent capacitance, C_d . C_d is a parallel combination of the diffusion capacitance C_{diff} of MOS devices. The drain-source resistance is ignored in the case of having large inverters.

The π structure of the RLC-π circuit makes the impedance calculations very simple. For instance, the diffusion capacitances of the driving CMOS circuits are placed directly in parallel with the capacitance, C_1 of the RLC-π circuitry and consequently no additional calculation is required.

The dissipated energy per period of this circuit is calculated for both the underdamped and the overdamped responses.

3.1.1. Underdamped response

In the underdamped case, the voltage and current transient waveforms oscillate toward their steady-state values. If $R_{int}<2\sqrt{L_{int,tot}/(C_2+C_3)}$ then the current and voltage waveforms will oscillate until they reach their steady state value. To obtain the total energy transferred out of the power supply Eq. (9) is used. The input current to the circuit is first obtained by solving the characteristic differential equation of the RLC-π circuit:

$$i_{DD}=(C+C_{eq,\pi})V_{DD}\delta(t)+\frac{V_{DD}}{L_{int,tot}\omega_{d,\pi}}\left(\frac{C_3}{C_2+C_3}\right)^2 e^{-\alpha_\pi t}\sin\omega_{d\pi}t \qquad (10)$$

where $C_{eq,\pi}=C_1+C_2 \circledS C_3$ is the equivalent capacitance of the RLC-π circuit. α_π, the damping constant, is $\alpha_\pi=R_{int}/2L_{int}$, $\omega_{p,\pi}$, the resonant frequency, is $\omega_{p,\pi}^2=1/(L_{int}(C_2+C_3))$, and $\omega_{d,\pi}$, the oscillation frequency, is $\omega_{d,\pi}^2=\omega_{p,\pi}^2-\alpha_\pi^2$. C_1, C_2, and C_3 are given by Eq. (6). $C_2 \circledS C_3$ represents the series combination of C_2 and C_3.

The total energy delivered by the power-supply is:

$$E_{u,step}^{xline}=(C_d+C_1+C_3)V_{DD}^2-\left(\frac{C_3^2}{C_2+C_3}\right)V_{DD}^2\left(\frac{\omega_{p,\pi}}{\omega_{d,\pi}}\right)e^{\frac{\alpha_\pi T}{2}}\sin\left(\frac{\omega_{d,\pi}T}{2}+\Phi_\pi\right) \qquad (11)$$

where $\Phi_\pi=\text{atan}(\omega_{d,\pi}/\alpha_\pi)$. Remember that $C_1+C_3=C_L+C_{int,tot}$. It is observed that if a CMOS inverter driving a lossy coupled line undergoes an underdamped oscillatory response, and if $R_{int}/L_{int,tot}>>4\pi f_{clock}$ (or equivalently if $1/(2\pi\sqrt{L_{int,tot}(C_2+C_3)})>>2f_{clock}$), then the energy expression becomes:

$$E_{u,step}^{xline}=(C_d+C_{int,tot}+C_L)V_{DD}^2 \qquad (12)$$

Equations (11) and (12) give the actual and steady-state energy dissipation per clock period, respectively, when the circuit experiences an underdamped oscillatory transient response.

❒

3.1.2. Overdamped response

In the overdamped case R_{int} is sufficiently large (i.e., $R_{int}>2\sqrt{L_{int,tot}/(C_2+C_3)}$) such that it eliminates the resonances from current and voltage waveforms. Once again, to obtain the total energy transferred out of the power supply using Eq. (9), the input current to the circuit is first obtained by solving the characteristic differential equation of the RLC-π circuit:

$$i_{DD}=(C_d+C_{eq,\pi})V_{DD}\delta(t)+\frac{V_{DD}}{L_{int,tot}\alpha_{d,\pi}}\left(\frac{C_3}{C_2+C_3}\right)^2 e^{-\alpha_\pi t}\sinh\alpha_{d\pi}t \qquad (13)$$

where $\alpha_{d,\pi}=\sqrt{\alpha_\pi^2-\omega_{p,\pi}^2}$. The total energy delivered by the power-supply for the overdamped transient response is:

$$E_{o,step}^{xline}=(C_d+C_1+C_3)V_{DD}^2-\left(\frac{C_3^2}{C_2+C_3}\right)V_{DD}^2\left(\frac{\omega_{p,\pi}}{\alpha_{d,\pi}}\right)e^{\frac{\alpha_\pi T}{2}}\sinh\left(\frac{\alpha_{d,\pi}T}{2}+\Psi_\pi\right) \qquad (14)$$

It turns out that if a CMOS inverter driving a lossy coupled line has an overdamped response, and if $\alpha_\pi-\alpha_{d,\pi}>>4\pi f_{clock}$, then the energy dissipation per each clock period is the same as Eq. (12).

Equations (12) and (14) give the steady-state and the actual energy dissipation per clock period, respectively, when the circuit experiences an overdamped transient response.

❒

Remember that the electrical parameters of the lossy transmission line are a function of the geometrical parameters of the line such as wire width, wire thickness and wire length. Similarly, C_d is a function of the MOS gate aspect-ratio. Using BSIM3v3 I-V equations for the MOS transistor and accurate closed form expressions derived in [6], the energy variations in terms of the geometrical parameters of the interconnect and MOS transistors are obtained. Fig. 5.a shows the energy variation as a function of the fundamental period, *T*, and under the five different gate aspect-ratios of the driver. Fig. 5.b shows the energy variation with respect to the clock period for the five different values of the metal widths of the interconnect. The input is a periodic rectangular voltage signal. Please note that for small clock periods, the $(1/2)CV^2$ energy model gives rise to a wrong value.

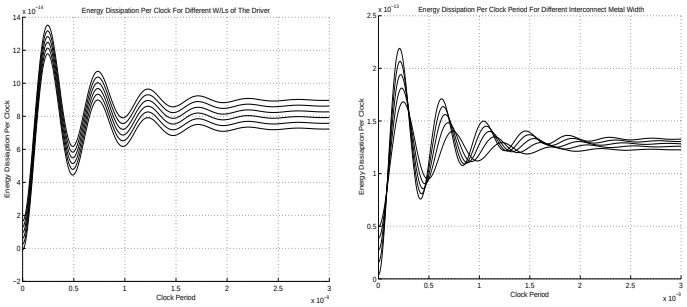


Fig. 5. (a) Energy per clock vs. clock period for six different W/L ratios (b) Energy per clock vs. clock period for four different interconnect widths (RLC-π)

As the metal width of the interconnect decreases, the variations of dissipated energy per clock period in terms of the clock period gradually changes from a damped oscillatory function to a growing exponential function. Please note that due to the large gate aspect-ratios, the overdamped response is rarely observed in the case of having large drivers. The same statement is true for the case when the W/L of the transistors decreases. Figures 5.a and 5.b suggest that for a given clock period, we can change the transistor as well as interconnect metal width such that the dissipated energy per clock period attains its undershoot value which is beneficial from both the speed and energy point of view.

To figure out the voltage variations across the load capacitance, the same circuit utilized and is excited by a step input. Figures 6.a and 6.b show the voltage waveform across the load capacitance for different values of interconnect widths and W/L ratios of the transistors of the driver, respectively.

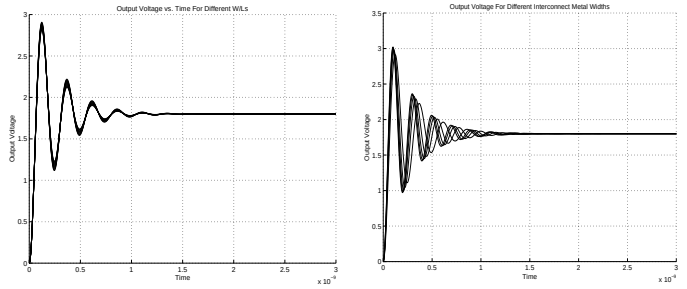


Fig. 6. (a) Voltage waveform for six different W/L ratios (b) Voltage waveform for four different interconnect widths (RLC-π)

Having accurate expressions for the energy dissipation of a lossy transmission line driven by CMOS drivers helps us propose a new design guideline for an area-efficient wire and transistor sizing to achieve the minimum energy under the noise-margin constraint. However, considering the energy dissipation alone is misleading. In other words, doing wire and transistor sizing to achieve the minimum energy may result in unacceptable delay and insufficient voltage swing, and as a result may lead to the logic and the circuit failures.

To take the effect of the circuit delay into account, we propose a new metric. For the overdamped response since all the waveforms are monotonically rising or falling waveforms, the best performance metric is the *energy-50% delay-product*. However, for the underdamped response the delay must incorporate the settling time of the oscillations as well as the percentage of maximum undershoot for noise-margin violations. To come up with a unique metric for both the underdamped and overdamped responses we use the *energy-50% delay.*(*1+undershoot%*)*-product* (*EDUP*). Fig. 7 shows the *EDUP* per clock cycle of an inverter driving a lossy transmission line with a pure capacitive load termination. Please note that for smaller W/L ratios as long as the condition given in (7) is valid, Fig. 7 can be used. The small incremental positive slope of the *EDUP* metric with respect to the W/L is due to the direct relationship between the energy and the diffusion capacitance of the device.

3.2. Energy calculation for lossy lines driven by small inverters

Now consider a lossy transmission line that is driven by a small inverter. If

the condition (8) is satisfied, then the lossy transmission line is modeled by the RLC circuit shown in Fig. 2.a. Similar to the previous section, we assume that a conducting transistor will be in the linear region for the entire input transition. In the case of small inverters, each transistor is modeled by an ideal switch in series with its drain-to-source resistance, r_{DS}. The MOS resistance gets in series with the RLC equivalent circuit.

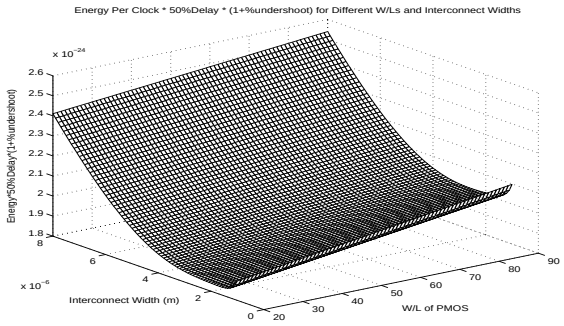


Fig. 7. *EDUP* in terms of W/L and interconnect metal width (RLC-π)

The dissipated energy per period of this circuit is calculated for both the underdamped and the overdamped responses.

3.2.1. Underdamped response

In the underdamped case, the voltage and current transient waveforms oscillate toward their steady-state values. This transient behavior occurs when $(R_{eq}+r_{DS}) < 2\sqrt{L_{eq}/(C_{int,tot}+C_L)}$. Calculating the current flowing out of the power-supply voltage and plugging it in Eq. (9) leads to the following expression for the dissipated energy:

$$E_{u,tot}^{RLC} = (C_{int,tot}+C_L)V_{DD}^2\left[1-\left(\frac{\omega_p}{\omega_d}\right)e^{\frac{\alpha T}{2}}\sin\left(\frac{\omega_d T}{2}+\Phi\right)\right] \quad (15)$$

where $\alpha = (R_{eq}+r_{DS})/2L_{eq}$, $\omega_p^2 = 1/L_{eq}(C_{int,tot}+C_L)$, $\omega_d = \sqrt{\omega_p^2-\alpha^2}$, and $\Phi = \text{atan}(\omega_d/\alpha)$. The effect of the diffusion capacitances of the driver is taken into account by simply adding C_d to the first parenthesis of Eq. (15). It is easily observed that the steady-state value of the dissipated energy per period is:

$$E_{u,tot}^{RLC} = (C_{int,tot}+C_L+C_d)V_{DD}^2 \quad (16)$$

❒

3.2.2. Overdamped response

In the overdamped case, the resistor is sufficiently large (i.e., $(R_{eq}+r_{DS}) > 2\sqrt{L_{eq}/(C_{int,tot}+C_L)}$) such that it eliminates the resonances from current and voltage waveforms. The total energy delivered by the input source is:

$$E_{o,tot}^{RLC} = (C_{int,tot}+C_L)V_{DD}^2\left[1-\left(\frac{\omega_p}{\alpha_d}\right)e^{\frac{\alpha T}{2}}\sinh\left(\frac{\alpha_d T}{2}+\Psi\right)\right] \quad (17)$$

where $\Psi = \text{atanh}(\alpha_d/\alpha)$. Similar to the underdamped response C_d is added to the first parenthesis of Eq. (17). Once again the steady-state value of the dissipated energy per period is the same as Eq. (16).

❒

Once again, using BSIM3v3 I-V equations for the MOS transistor and accurate closed form expressions derived in [6], the energy variation in terms of the geometrical parameters of the interconnect and MOS transistors are obtained. Fig. 8.a shows the energy variations as a function of the fundamental period, *T*, and under the five different gate aspect-ratios of the driver for the equivalent RLC circuit. Fig. 8.b shows the energy variation with respect to the clock period for the five different values of the metal widths of the interconnect. The input is a periodic rectangular voltage signal. Please note that for small periods, the $(1/2)CV^2$ energy model gives rise to a wrong value.

Figures 9.a and 9.b show the voltage waveform across the load capacitance for different values of interconnect widths and W/L ratios of the transistors of the driver, respectively.

Like the previous section, considering the energy dissipation alone to propose new design guidelines is misleading. To take the effect of the circuit delay into account, we propose a new metric, *the energy-50% delay.(1+undershoot%)-product* (*EDUP*). Fig. 10 shows the variation of the *EDUP* in terms of the interconnect width and PMOS W/L ratio. The *EDUP* is an increasing function of the W/L ratio for larger values of the W/L. For large values of W/L ratios, as long as the condition given in (8) is satisfied the formulations of this section and the plot in Fig. 10 is valid. For larger values of W/L ratios, the RLC-π circuit must be used and therefore Fig. 7 must be utilized.

4. CONCLUSION

This paper presented accurate closed-form expressions for the energy dissipation of lossy transmission lines driven by CMOS drivers. The energy was calculated using approximated expressions for the driving-point impedance of a lossy transmission line. A comprehensive analysis was incorporated to derive the dissipated energy of a lossy transmission line. Moreover, a new design metric, the EDUP metric, was proposed that is very relevant for the energy optimization under the delay constraint. Several experimental results show the accuracy of our approach.

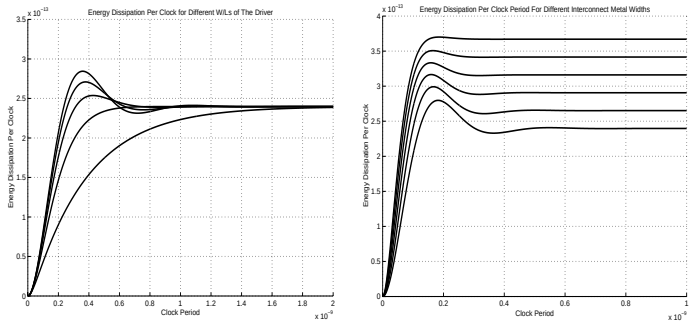


Fig. 8. (a) Energy per clock vs. clock period for five different W/L ratios (b) Energy per clock vs. clock period for six different interconnect widths (RLC)

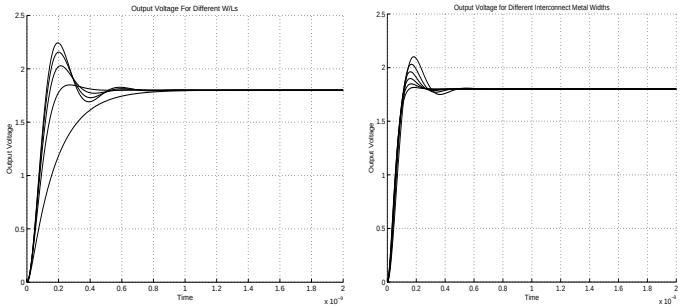


Fig. 9. (a) Voltage waveform for five different W/L ratios (b) Voltage waveform for four different interconnect widths (RLC)

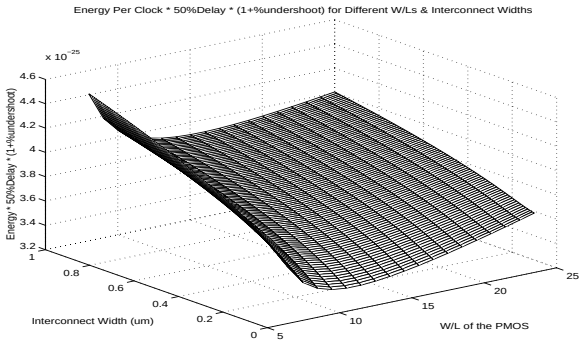


Fig. 10. *EDUP* in terms of W/L and interconnect metal width (RLC)

5. REFERENCES

[1] T. Uchino, J. Cong, "An Interconnect Energy Model Considering Coupling Effects," *Proceedings of IEEE/ACM Design Automation Conference*, pp. 555-558, Las Vegas, June 2001.

[2] C. N. Taylor, S. Dey, Y. Zhao, "Modeling and Minimization of Interconnect Energy Dissipation in Nanometer Technologies," *Proceedings of IEEE/ACM Design Automation Conference*, pp. 754-757, Las Vegas, June 2001.

[3] J. A. Davis, R. Venkatesan, A. Kaloyeros, M. Beylansky, S. J. Souri, K. Banerjee, K. C. Saraswat, A. Rahman, R. Reif, and J. D. Meindl, "Interconnect Limits on Gigascale Integration (GSI) in the 21st Century," *Proceedings of the IEEE*, *Special Issue on Limits of Semiconductor Technology*, Vol. 89, No. 3, pp. 305- 324, March 2001.

[4] A. Deutsch, P. W. Coteus, G. Kopcsay, H. Smith, C. W. Surovic, B. Krauter, D. Edelstein, P. Restle, "On-chip Wiring Design Challenges for Gigahertz Operation," *Proceedings of the IEEE*, Vol. 89, No. 4, pp. 529- 555, April 2001.

[5] S.-M. Kang, Y. Leblebici, *CMOS Digital Integrated Circuits Analysis and Design*, pp. 196-204, McGraw-Hill Companies, Inc., 1999.

[6] http://www-device.eecs.berkeley.edu/~bsim3/get.html