A 22–29-GHz UWB Pulse-Radar Receiver Front-End in 0.18-μm CMOS

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***Abstract*—The design of a CMOS 22–29-GHz pulse-radar receiver (RX) front-end for ultra-wideband automotive radar sensors is presented. The chip includes a low-noise amplifier, in-phase/quadrature mixers, a quadrature voltage-controlled oscillator (QVCO), pulse formers, and baseband variable-gain amplifiers. Fabricated in a 0.18-μm CMOS process, the RX front-end chip occupies a die area of 3 mm^2. On-wafer measurements show a conversion gain of 35–38.1 dB, a noise figure of 5.5–7.4 dB, and an input return loss less than -14.5 dB in the 22–29-GHz automotive radar band. The phase noise of the constituent QVCO is -107 dBc/Hz at 1-MHz offset from a center frequency of 26.5 GHz. The total dc power dissipation of the RX including output buffers is 131 mW.**

***Index Terms*—CMOS, direct-conversion receiver (RX), integrated circuits, low-noise amplifier (LNA), pulse radar, quadrature voltage-controlled oscillator (QVCO), ultra-wideband (UWB).**

I. Introduction

LOW-COST implementation of automotive radars is a cornerstone in the development of intelligent transportation systems. Long-range radars enabling adaptive cruise control (ACC) have been around for some time in luxury-class vehicles [1]. These radars have a typical range of >150 m and a range resolution on the order of 1 m. Short-range radars providing a high-resolution safety zone around the vehicle are essential for incorporating advanced driver-assistance and security functions including collision avoidance, precise airbag activation, parking assistance, blind-spot detection, lane change support and short-range ACC stop-and-go capability. Several of these functions require detection of objects at distances ranging from 10 cm to 40 m, and a radar range resolution of only a few centimeters, necessitating ultra-wideband (UWB) operation [2].

Short-range sensors demand high range resolution radars, entailing the use of narrow pulses, and thus wide signal bandwidth. An important factor in the development of such radar systems is thus a contiguous spectrum allocation by regulatory agencies worldwide. Frequency bands around 24 GHz have been allocated in both the USA and Europe, exclusively for UWB vehicular radars. For example, the Federal Communications Commission (FCC) has allocated an unlicensed 7-GHz-wide spectrum between 22–29 GHz with strict emission restrictions [3].

These allocations have instigated intensive research and development, by both academia and industry, to develop vehicular radar sensor systems. Realization of 22–26-GHz short-range radar transceiver circuits has been reported in a silicon–germanium (SiGe) process [2], [4], but suffers from limited integration, limited bandwidth, and high power dissipation. Since small form factor and low cost are imperative for automotive applications, a *pure* CMOS implementation is attractive and can make radar sensors affordable to the end customer. Recent works have demonstrated the possibility of designing highly integrated high-frequency circuits in advanced CMOS technologies [5]–[8]. While *narrowband* 24-GHz silicon-based (SiGe and CMOS) transceivers for high data-rate wireless communications have been reported in prior work [9], [10], the realization of truly *wideband* automotive radar circuits in CMOS technologies was first explored in [7] and [8].

This paper presents the detailed design and analysis of a CMOS short-range automotive pulse-radar receiver (RX) front-end operating in the UWB band from 22 to 29 GHz. Various design techniques are introduced in order to boost circuit performance at frequencies around only half of the transit (or unity current gain) frequency f_T of the transistor ($f_T \approx 55$ GHz for 0.18-μm CMOS). An interference-reduction scheme is also presented that allows efficient use of the allocated power-constrained spectrum, while minimizing the interference with other systems operating in the same frequency range. Circuit techniques used in the UWB RX front-end design enable the radar sensor to potentially achieve a high-range resolution and detect objects at a close range, thereby demonstrating suitability for integration in short-range radar systems.

This paper is organized as follows. Section II briefly reviews the 22–29-GHz spectrum. Section III discusses the architecture of the radar RX. Section IV describes the circuit design of the building blocks of the front-end. Measurement results are presented in Section V. Finally, Section VI provides concluding remarks.

II. Overview of the 22–29-GHz UWB Spectrum

Although this study presents the RX front-end of the UWB pulse radar, an overview of the regulations is deemed necessary to understand design requirements of the RX and high-frequency pulse-generation circuitry. Fig. 1(a) shows the spectral masks for various systems that operate between 22–29 GHz. Although the 7-GHz bandwidth allocated by the FCC enables significant improvement of range resolution, short-range automo-

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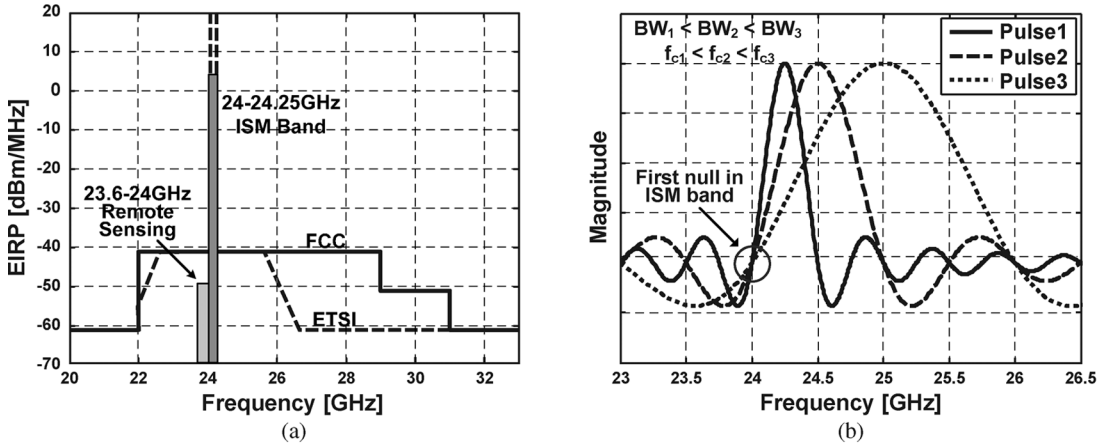


Fig. 1. (a) Spectrum allocations for systems operating in the 22–29-GHz band (EIRP = Effective Isotropic Radiated Power). (b) Pulse-bandwidth (BW) dependent carrier frequency (f_c) ensures minimum emission in the ISM band located at 24.125 GHz.

tive radar systems in this band are constrained by low transmit power levels. The spectral density of the average transmitted signal should not exceed -41.3 dBm/MHz in this band [3]. Moreover, as is clear from Fig. 1(a), the operating frequency band overlaps with existing systems around 24 GHz. For instance, narrowband phased-array transceivers suitable for wireless data communication reported in [9] and [10] operate in the unlicensed 24.125-GHz industrial, scientific, and medical (ISM) band. The FCC also stipulates a center frequency above 24.075 GHz with limited emissions in the 23.6–24.0-GHz band in order to strongly minimize interference with remote sensing and radio astronomy equipment operating in this band.

In compliance with the above FCC regulations, the local oscillator (LO) circuitry in this work, described in Section IV-C, has been designed for a nominal center frequency of 26.5 GHz and a tuning range from 24.5 to 28.5 GHz. Furthermore, this choice of tuning range facilitates the use of a digital signal processing (DSP) algorithm, which sets the control voltage (and hence, the oscillation frequency) of the oscillator, such that the first null of the sinc spectrum of a radar pulse falls in the aforementioned restricted band, thereby reducing unwanted emissions [2]. This idea is illustrated using MATLAB simulations in Fig. 1(b). As the pulse bandwidth increases, the carrier frequency is appropriately increased such that the first null stays in the ISM band.

FCC spectral occupancy limitations [3] and a range-resolution requirement of less than 5 cm [2] result in signal main-lobe (null-to-null) widths of around 10 GHz. Note that the FCC defines the bandwidth of a UWB signal as the frequency band bounded by the -10-dBc points of its spectrum. The 10-GHz null-to-null spectral width will, therefore, result in approximately an 8-GHz FCC signal bandwidth. In combination with the fact that the rise and fall times ($\sim$50 ps) of the UWB pulses are not negligible compared to the pulsewidths, this implies that pulses as short as 200 ps are needed to occupy the entire FCC bandwidth.

The pulse repetition frequency (prf) is given by

$$\text{prf} = \frac{c}{2R} \tag{1}$$

where c is the speed of light and R is the minimum unambiguous radar range. Using (1), a minimum unambiguous radar range of 40 m results in a prf of 3.75 MHz. It is important to note that in order to meet the FCC average power emission requirements, either the prf or the pulse power must be decreased. A longer pulse can be transmitted with higher total pulse energy, resulting in a higher signal-to-noise (SNR). This would require a reduction in prf and the use of pulse compression (e.g., binary phase-shift keying (BPSK) and PN coding) in order to meet the spectral limitations and to achieve the same range resolution as a short pulse. Nevertheless, the pulsewidth cannot be arbitrarily increased due to the peak power emission restrictions.

III. RX Architecture

Several radar architectures have been studied and employed in the past (see [11] and [12]). The choice of architecture for short-range radars is governed by the requirements of high-range resolution, close-range detection, and wide dynamic range. PN-coded radars and pulsed radars are the two most suitable architectures for meeting these requirements. Frequency-chirped radars are difficult to implement for UWB bandwidth in excess of 1 GHz due to the challenge of generating a wideband low phase-noise chirp in CMOS technologies. A recently published SiGe frequency synthesizer for 76-GHz long-range radars [13] exemplifies the level of complexity involved in meeting the phase-noise requirements of frequency-chirped radars. PN-coded radars are resilient to interference, but suffer from limited range due to poor isolation between the RX and transmitter (TX) and limited dynamic range [2]. Pulse radars, on the other hand, can attain a high dynamic range as the RX and TX operate in a time-duplexed fashion. Higher dynamic range directly translates to improved range of the radar sensor, as objects at farther distances can be detected. The rather low complexity of the pulsed-radar architecture makes it well suited for UWB 22–29- and 76–81-GHz millimeter-wave short-range radars.

In light of the aforementioned advantages, the proposed RX is based on a pulse-radar architecture. In order to understand the radar operation, consider the conceptual block diagram of a pulse-radar transceiver shown in Fig. 2 [2]. The pulsewidth

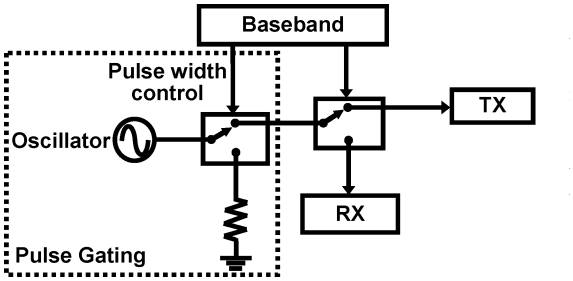


Fig. 2. Conceptual operation of a pulsed-radar transceiver [2].

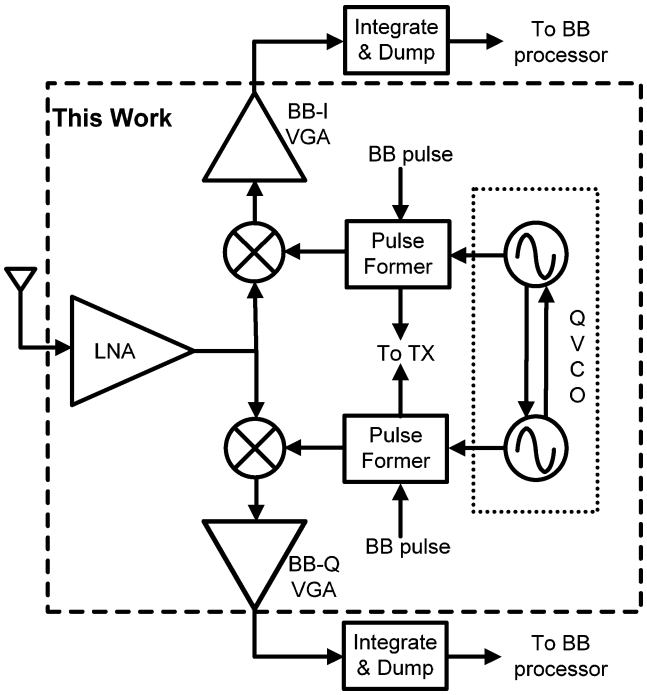


Fig. 3. Block diagram of the UWB pulse-radar RX front-end.

control signal gates the sinusoid from the oscillator to generate a high-frequency gated sine wave, which is then transmitted by the TX. This triggers a baseband (BB) delay circuitry, which waits for a certain time until another trigger is enabled. At the second trigger, the second switch is changed from the TX to RX. The RX then samples its output at this instant. Thus, the input from the RX antenna is multiplied with a replica of the transmitted pulse. If the two pulses do not overlap in time, the output will be zero, whereas if they are coincident, the output will be a maximum. The delay between the two triggers determines the range gate being scanned at the time. Thus, by changing this delay, objects at varying distances can be detected. Due to output power limitations and several other factors such as clutter, system losses, and interference [11], [14], a single-pulse SNR turns out to be negative for the desired range, and hence, several received pulses need to be integrated to detect an object.

The proposed RX employs time-gated quadrature correlation architecture, as shown in Fig. 3. Essentially a direct-conversion architecture, this pulse-radar RX front-end is comprised mainly of the following:

1) 22–29-GHz UWB low-noise amplifier (LNA);
2) in-phase/quadrature (I/Q) mixers;
3) quadrature voltage-controlled oscillator (QVCO);
4) high-isolation pulse formers;
5) BB variable-gain amplifiers (VGAs);
6) wideband integrate-and-dump circuits.

The UWB LNA amplifies the received wideband RF pulses with minimal magnitude- and phase-distortion. I/Q mixers correlate the amplified RF pulses with locally generated pulses (delayed replicas of the transmitted pulses) from the pulse formers. A free-running injection-locked QVCO generates I and Q differential LO signals, which are fed to the pulse formers through high-frequency tuned buffers. The pulse formers upconvert the BB pulses to the vehicular-radar band by modulating them on the 26.5-GHz (nominally) LO I/Q carriers. The cross-correlation products are then amplified by the BB VGAs and fed to integrate-and-dump circuits for BB processing. Note that the pulse generator and integrate-and-dump circuitry are not included, and are being developed as a continuation of this work.

IV. Circuit Design

In addition to the numerous system-level issues discussed in Section III, UWB radars present several circuit-design issues. Particularly, obtaining a wide bandwidth with adequate circuit performance across the entire 22–29-GHz band is challenging. This is exacerbated by the limited gain of 0.18-μm MOS transistors, with f_T of 55 GHz, over this desired range of frequencies. In this section, several circuit topologies for the critical building blocks of the proposed RX front-end are presented to address the UWB challenges. The circuits have been designed for a bandwidth of 7 GHz to maximize the achievable range, and to allow for process variations and design margins.

A. 22–29-GHz UWB Neutralized LNA

Fig. 4 shows the schematic of the UWB LNA comprised of two common-source amplifier stages employing wideband impedance matching and $C_{\rm GD}$ neutralization. Source degeneration with inductor L_s is used in the first stage for impedance matching and linearity improvement, but not in the second stage so as to achieve sufficient gain. Each stage employs a feedback path consisting of a center-tapped inductor (L_4/L_6) and a MOS capacitor (C_{n1}/C_{n2}) to counteract the detrimental effects of the gate–drain capacitance $C_{\rm GD}$ on the frequency response and to guarantee the stability of the amplifier [15]. The center-tapped inductor (L_4/L_6) generates a phase-difference of 180° between its two terminals due to which the current flowing through the neutralization capacitor (C_{n1}/C_{n2}) is equal and opposite to that flowing through $C_{\rm GD}$. MOS capacitors are used to realize the neutralization capacitors because they compensate (to the first order) for the voltage and process dependence of $C_{\rm GD}$, thereby improving the neutralization accuracy. This technique ensures a stable amplifier, while eliminating the high-frequency noise and bandwidth degradation associated with a cascode LNA. This, in turn, yields a better noise figure (NF) and gain rolloff than the widely used cascode LNA. Intuitively, the NF of the LNA in this work is better than a cascode LNA because it utilizes only one transistor per stage in the signal path. Moreover, at high frequencies, the parasitic inductance of the bypass capacitor connected to the gate of a cascode device can degrade the stability factor of the amplifier [16].

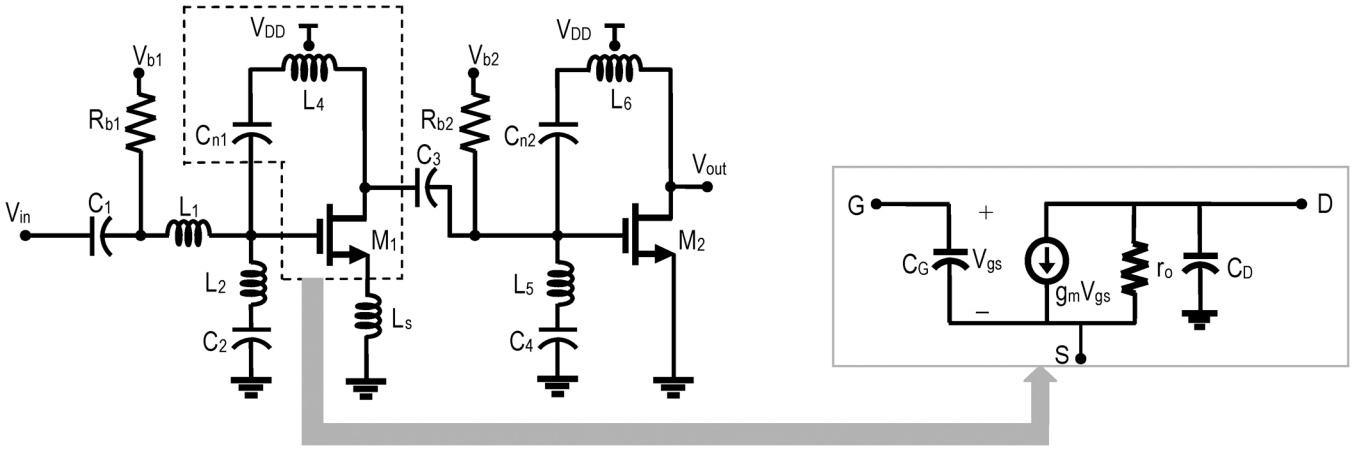


Fig. 4. Schematic of the UWB LNA with a simplified small-signal model of the first stage transistor.

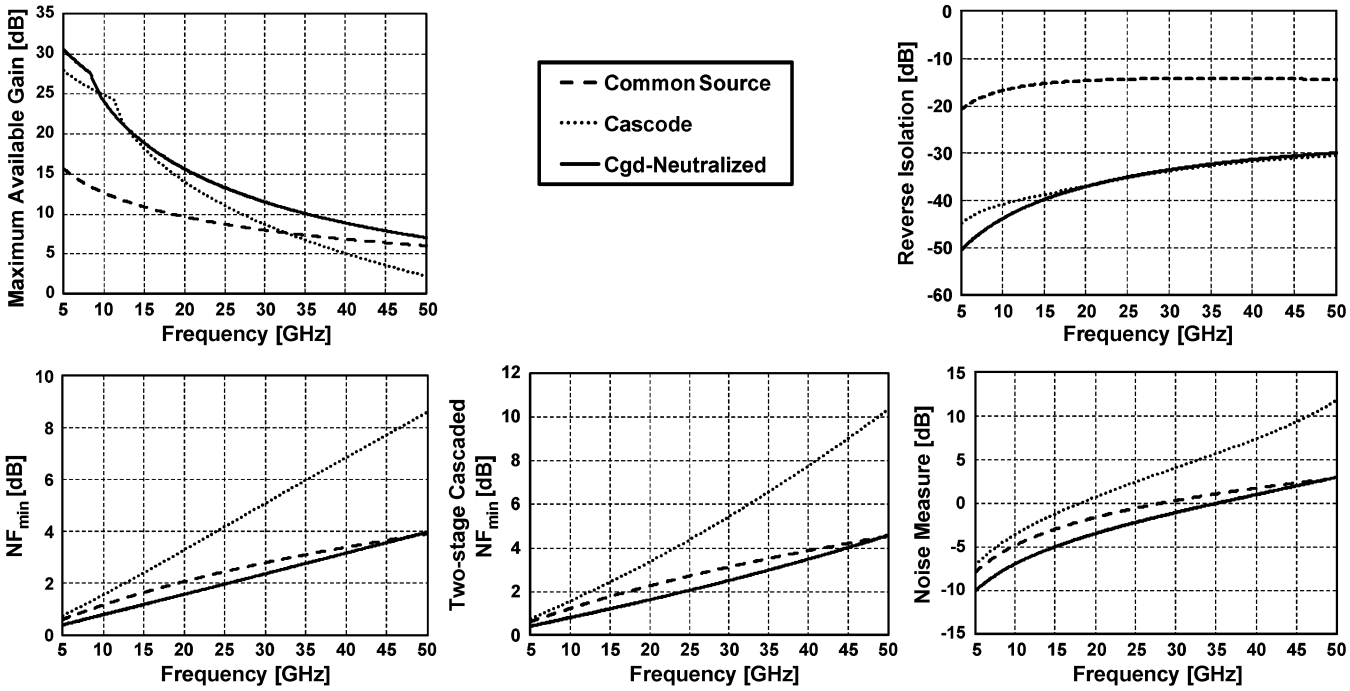


Fig. 5. Comparison of maximum available gain, reverse isolation, and minimum NF and noise measure for various LNA topologies.

Simulation data comparing the behavior of minimum NF, gain, and reverse isolation with respect to frequency for common-source, cascode, and perfectly neutralized amplifier stages are shown in Fig. 5. As is evident from this figure, a $C_{\rm GD}$-neutralized stage provides higher gain and lower minimum NF than both common-source and cascode amplifiers, while achieving reverse isolation as good as that of a cascode stage. The suitability of an amplifier to be used in a multistage amplifier can be ascertained by determining its noise measure M given by [17]

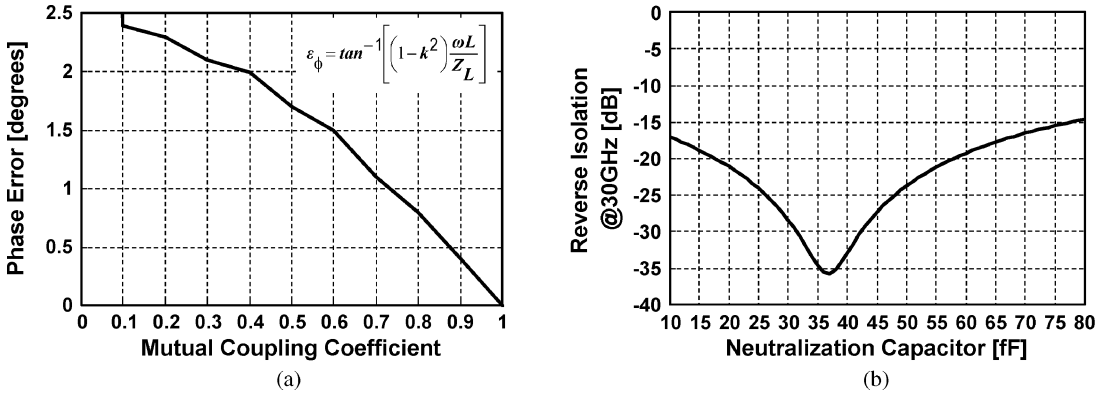
$$M = \frac{F-1}{1-\dfrac{1}{G_A}} \tag{2}$$

where F is the noise factor and G_A is the available gain of the amplifier. Due to its higher available gain and lower minimum NF, the neutralized stage has a lower noise measure than both common-source and cascode stages, as shown in Fig. 5.

Since correct operation of the neutralized amplifier depends on the cancellation of $C_{\rm GD}$, it is important to investigate the sources of imperfect cancellation and their impact on the circuit performance. One source of error originates from the center-tapped inductor itself, namely, the imperfect coupling factor, i.e., $k < 1$, between the two halves. A nonunity coupling factor results in a deviation from the ideal 180° phase difference at the inductor terminals. Using the circuit analysis of the LNA, the phase error ε_ϕ can be expressed as

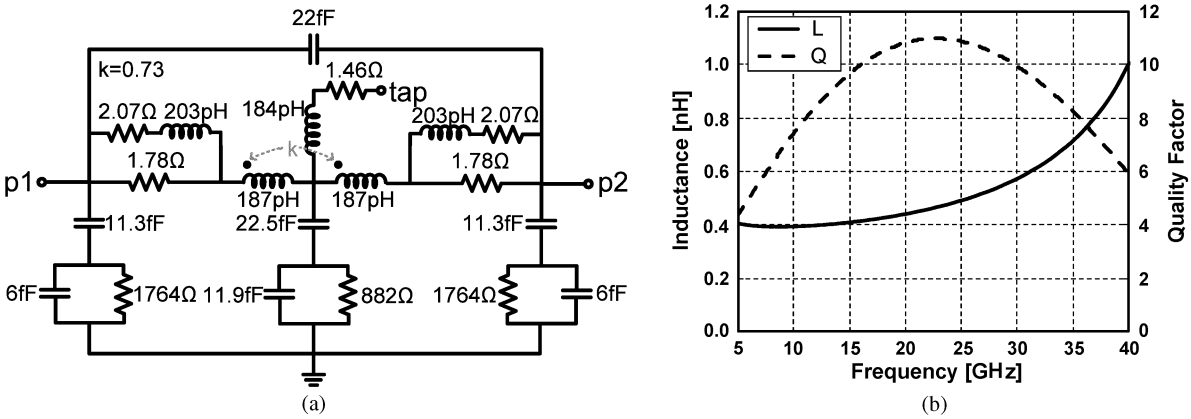
$$\varepsilon_\phi = \tan^{-1}\left[(1-k^2)\frac{\omega L}{Z_L}\right] \tag{3}$$

where L is the half-inductance of the center-tapped inductor and Z_L is the load impedance seen by the inductor at the amplifier's drain terminal. The change in phase error as a function of k is shown in Fig. 6(a) indicating negligible phase error due to imperfect coupling. For the center-tapped inductors used in the



(a) (b)

Fig. 6. Sources and effects of imperfect neutralization. (a) Phase error at the center-tapped inductor terminals as a function of the mutual coupling. (b) Reverse isolation of a $C_{\rm GD}$-neutralized stage at 30 GHz with varying neutralization capacitor; $C_{\rm GD} \approx 35$ fF.



(a) (b)

Fig. 7. (a) Broadband model of the center-tapped inductors extracted from EM simulations. (b) Simulated half-inductance and Q.

LNA, a k of 0.73 was extracted from electromagnetic (EM) simulations. The extracted broadband model of the center-tapped inductors is shown in Fig. 7(a), where element values are obtained from EM simulations. The EM-simulation result of the inductance and its quality factor with respect to frequency are shown in Fig. 7(b).

Another source of imperfect cancellation is the variation in the neutralization capacitor caused by process/temperature variations and layout parasitics. While using a MOS capacitor to realize the neutralization capacitance reduces the effects of these variations, adequate tolerance to these variations is essential for robust circuit operation. Fig. 6(b) shows the effect of variations in neutralization capacitance on reverse isolation of the amplifier at 30 GHz (upper corner of frequency band of interest) with $C_{\rm GD} \approx 35$ fF. Even with more than 60% deviation from the optimum value of the neutralization capacitor, the reverse isolation is still better than that of a common source amplifier, demonstrating the robustness of the cancellation technique.

It turns out that the presented neutralization technique is inherently broadband and largely independent of frequency. However, in an RF LNA, another constraint, namely, impedance matching, must be taken into account. While this $C_{\rm GD}$-neutralization technique does not affect the input match, it affects the output impedance of the common-source amplifier. In order to decouple neutralization and matching constraints, the output matching network is first designed to cancel the reactive part

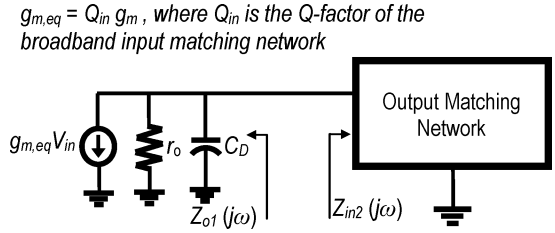


Fig. 8. Small-signal equivalent circuit at the output of the LNA's first stage.

of the transistor output impedance, which sets the value of the neutralization inductor as a part of this matching network (cf. Fig. 8). The inductor is then converted to a center-tapped transformer with the same half-inductance. A neutralization capacitance value is then readily found, which completes the design.

Wideband power match is essential at the input of the LNA for maximizing power gain across the entire signal bandwidth. To this end, a third-order elliptic bandpass filter (BPF) network has been designed at the LNA input port. The BPF includes the source-degeneration inductor L_s and resonates out the reactive component of the LNA input impedance over the entire 22–29-GHz bandwidth, thus providing a wideband 50-Ω input match. The initial BPF network was readily obtained by bandpass transformation of a third-order Cauer (or elliptic)

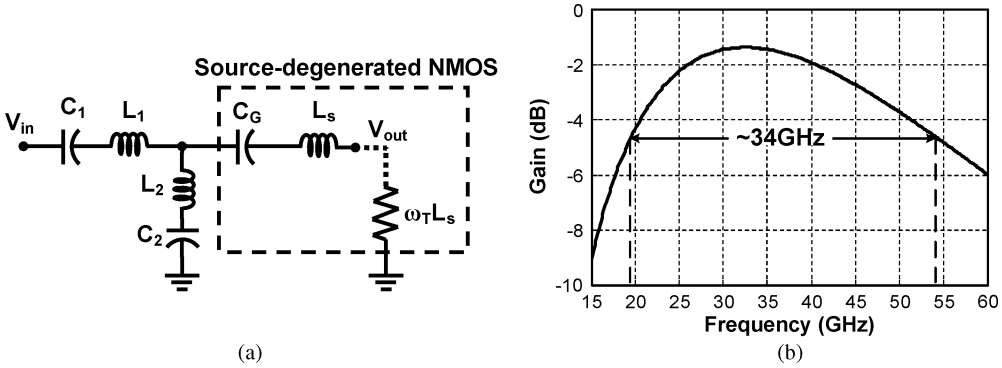


Fig. 9. (a) Equivalent third-order Cauer BPF matching network at the input of the LNA. (b) Its simulated frequency response.

low-pass filter. The network with actual device models was then optimized using simulations. A Cauer implementation is proven to be order-efficient [18], and hence, the designed BPF requires fewer passive elements than an equivalent Butterworth or Chebyshev implementation (such as the one used in the 3.1–10.6-GHz LNA in [19]) for a given set of filter characteristics. The equivalent Cauer BPF is shown in Fig. 9(a) and the simulation of the standalone BPF exhibits a passband 3-dB bandwidth of 34 GHz, as shown in Fig. 9(b). Furthermore, although an elliptic filter can be designed to obtain a superior transition-band response, an attempt has been made here to reuse the same components to realize the filter and the neutralization. Therefore, gain rolloff is not given a high priority. Note that the dc blocking capacitors C_1 and C_2, both 950 fF, are part of the wideband matching network.

The feedback path elements in the second stage along with the *LC* section $L_5 - C_4$ constitute the inter-stage matching network in the LNA. The first stage is optimized for minimum NF, while the second stage is designed to be the major contributor to the overall power gain.

The use of common-source stages and inductive degeneration improves the linearity of the LNA, hence reducing distortion of the UWB pulses. The LNA achieves a peak power gain of 18 dB, input-referred 1-dB compression point of -7.2 dBm, and an NF less than 6 dB across the 22–29-GHz band.

To verify the superior performance of the proposed LNA compared to the cascode topology, and to prove guaranteed stability, a circuit analysis of the LNA is presented in the following.

Assuming perfect cancellation of $C_{\rm GD}$ using the neutralization technique $C_{\rm GD}$, the neutralization capacitor C_{n1} and the center-tapped inductor are removed from the small-signal circuit model, shown in Fig. 4. Thus, the gain of the neutralized stage is $A_v = -g_{m,\rm eq}(r_o \| Z_L)$, where $g_{m,\rm eq} = Q_{\rm in} g_m$ is the equivalent transconductance of the amplifier, $Q_{\rm in}$ is the Q factor of the input matching network, Z_L is the load impedance including the drain capacitance C_D, and r_o is the output resistance of the transistor. The small-signal model of the first stage of the LNA with the above simplifications is shown in Fig. 4.

Considering only the drain current noise, the NF of the neutralized LNA can be shown to be

$$F_1 = 1 + \frac{\left(Y_s^2 + \omega^2 C_G^2\right)\gamma g_{d0} R_s}{g_m^2} \tag{4}$$

where Y_s is the source admittance, R_s is the source resistance, ω is the operating angular frequency, γ is the technology-dependent excess noise parameter [15], and g_{d0} is the drain–source conductance at zero drain–source voltage.

On the other hand, in a cascode LNA, the extra common-gate transistor contributes additional noise, resulting in an overall NF of

$$F_2 = F_1 + \frac{\omega^2 (C_{G1} + C_{G2})^2 \left(Y_s^2 + \omega^2 C_{G1}^2\right)\gamma g_{d02} R_s}{g_{m1}^2 g_{m2}^2} \tag{5}$$

where C_{G2}, g_{m2}, and g_{d02} are the corresponding parameters of the cascode transistor. Due to the $C_{\rm GD}$ neutralization, the NF of the neutralized LNA approaches that of a common-source amplifier with $C_{\rm GD}$ ignored. Detailed analyses of the common-source LNA can be found in [19] and [20].

A major noise source that becomes significant at high frequencies is the induced gate noise [15] resulting from the capacitive coupling of the gate to channel fluctuations and noise. With the aid of an analysis introduced in [21] and taking into account the gate-induced noise and noise contribution of the physical gate resistance, the NF of the LNA without neutralization is obtained as (6), shown at the bottom of the page, where $C_{{\rm GD},M} = (1 + g_m r_o) C_{\rm GD}$ is the Miller equivalence of gate–drain overlap capacitance, r_G is the gate physical resistance, c is the correlation coefficient between gate and drain noise currents [15], and $\kappa_c = |c|\sqrt{\delta/(5\gamma)}$ (where δ is the gate

$$F_1' = 1 + \frac{r_G}{3R_s} + \frac{\gamma g_{d0}\left[\left\{\left(\frac{1}{|c^2|} - 1\right)\kappa_c^2 + \left(\frac{C_{{\rm GD},M}}{C_G} + \kappa_c + 1\right)^2\right\}\left\{\omega\left(\frac{r_G}{3} + R_s\right)C_G\right\}^2\right]}{g_m^2 R_s} \tag{6}$$

noise coefficient, a technology-dependent constant [15]). From (6), it is observed that the contribution of induced gate noise to the total NF becomes noticeable at high frequencies and with increasing gate–drain capacitance. The neutralization technique in the LNA, therefore, effectively reduces the $C_{\rm GD}$ effect, leading to an NF even better than the common-source amplifier, as also seen in simulations in Fig. 5.

Since the neutralized LNA relies on proper frequency-dependent feedback, its stability must be examined. A common-source amplifier becomes unstable at operating frequencies close to a significant fraction (dependent on foundry technology and transistor layout) of the transistor f_T. This is because the gate–drain capacitance provides undesirable positive feedback between the input and output, inducing oscillations in the circuit. The LNA demonstrated in this study, on the other hand, does not suffer from any such instability, owing to the $C_{\rm GD}$ cancellation technique. The real part of the input impedance of the neutralized LNA is obtained as

$$\mathrm{Re}\,[Z_{\rm in}(\omega)]=\frac{(r_o+\mathrm{Re}[Z_L])^2+\omega^2L_s^2}{\omega^2L_sC_G\,(r_o+\mathrm{Re}[Z_L])\,(\omega^2L_sC_G+g_mr_o)}. \tag{7}$$

Load impedances are typically on the order of tens of ohms in high-frequency CMOS amplifiers. Therefore, as readily ascertained from (7), the real part of the input impedance is positive for all frequencies and the amplifier stability is guaranteed. Furthermore, as expected, no stability problems were observed in simulations as well as measurements. The bulk terminal of each transistor in the amplifier is connected to the source, thereby eliminating the body effect and avoiding bandwidth degradation caused by the source-to-bulk capacitance. Although the drain–bulk capacitance affects the input impedance because of the feedback from source to gate, its contribution to bandwidth degradation at high frequencies is negligible due to the Miller effect [19].

B. Quadrature Mixers and BB VGAs

Two single-balanced mixers operating in quadrature mode correlate the amplified RF pulse (from the LNA) with local delayed replicas of the transmitted pulse. The schematic of one of the mixers is shown in Fig. 10, with the other mixer exactly the same. The amplified pulse is applied at the RF port, while the local pulse drives the LO port. PMOS active loads are used to increase the conversion gain while maintaining a 3-dB bandwidth of about 3.5 GHz in each of the I and Q paths. The output load of the LNA (L_6, r_{o2}), the mixer input network (C_b, L_g, L_s), and $C_{\rm GD1}$ and L_d form a wideband matching network between the LNA and mixer.

L_s also boosts mixer linearity as it provides a local series feedback path, but with accompanying reduction in gain. Besides participating in the impedance match at the mixer input, L_d enhances the RF transconductance's bandwidth by providing high-frequency isolation of the drain of M_1 from the noisy common source node of switch-pair $M_2 - M_3$. It also improves the impedance match at the LO port, where the switching transistors essentially operate in a common-source fashion at the switching instants. Each mixer is followed by a BB (0–3.5-GHz bandwidth) differential amplifier with variable

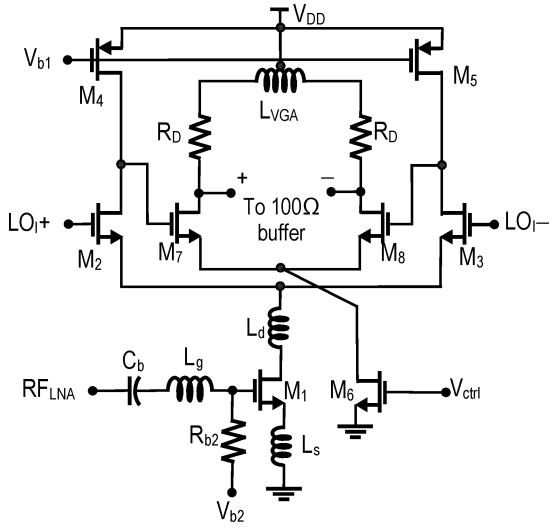


Fig. 10. Schematics of the mixer and VGA.

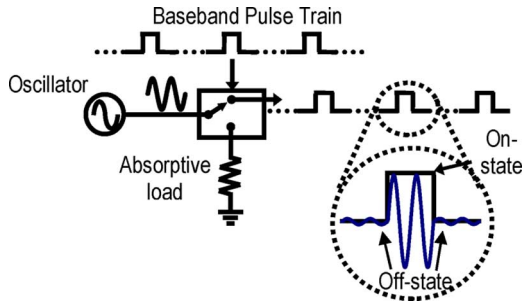


Fig. 11. Conceptual operation of the high-frequency pulse generation circuitry [22].

broadband gain of up to 10 dB controlled by the tail current of the amplifier. Shunt peaking [15] optimized for maximally flat group delay is employed to enhance VGA bandwidth and to ensure minimum distortion of the BB pulses at the output of the amplifier. Differential topology is used for the VGA to improve IIP_2 of the RX. BB outputs are taken off-chip through doubly terminated 100-Ω differential buffers for differential measurements using standard 50-Ω equipment. The mixers and VGAs draw a total of 20 mA, while the output buffers draw 21 mA from a 1.8-V supply.

C. Pulse Formation

One of the most critical building blocks of the radar RX presented in this study is the pulse generation circuitry. The conceptual operation of the LO pulse generation circuit is illustrated in Fig. 11 [22]. An oscillator generates a sinusoidal signal, which is either directly passed to the output when the BB pulse is high, or directed into an absorptive load when the BB pulse is low. As shown in this figure, the envelope of the output is ideally the same as the BB pulse. It is also apparent that due to finite isolation of the conceptual single-pole double-throw switch, part of the sinusoid leaks to the output even when the switch is in its off state.

It is readily inferred from the previous sections that an LO with a wide tuning range (24.5–28.5 GHz) and with quadrature

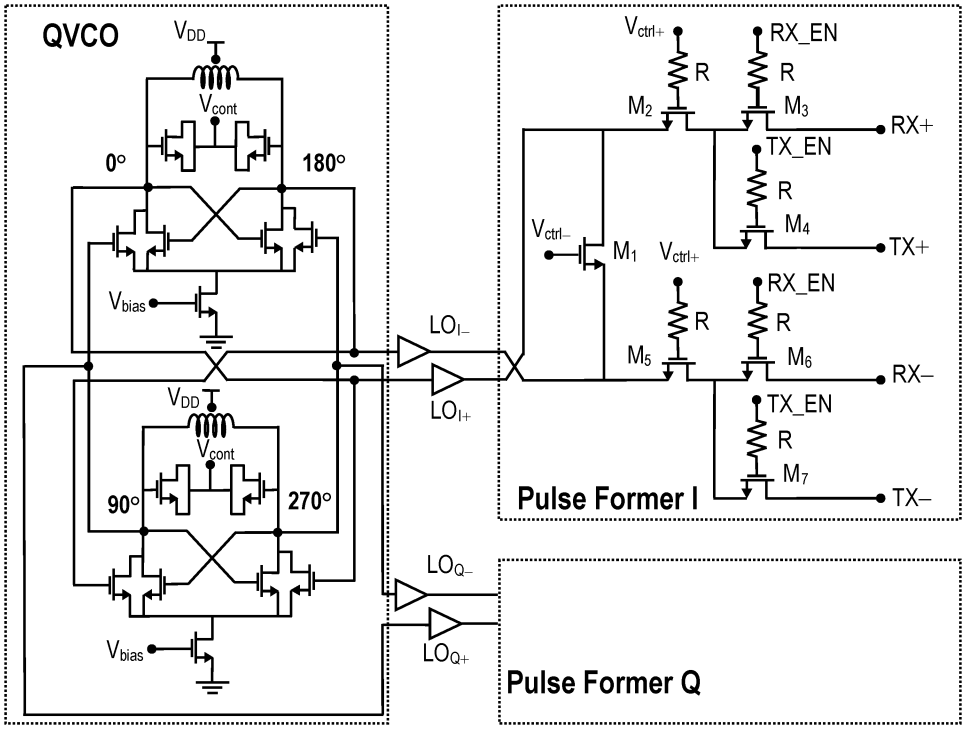


Fig. 12. Schematics of the QVCO and pulse formers.

outputs is needed. This is accomplished by employing an injection-locked QVCO, first presented in [23]. For convenience, the circuit schematic of the QVCO is shown in Fig. 12. The QVCO consists of two cross-coupled *LC* VCOs with injection-locking signals provided through coupling transistors to establish quadrature relationship between the differential outputs of the two VCOs. The phase relationship between the VCO outputs is illustrated in Fig. 12. Frequency tuning is achieved through accumulation-mode MOS varactors, with variable capacitance controlled by an external voltage $V_{\rm cont}$. The outputs of the VCOs are buffered to the pulse formers through high-frequency buffers. These tuned amplifiers shield the VCO circuits from the switching effects of the pulse formers, thereby reducing frequency pulling. The center-tapped spiral inductor in the VCO tank is 495 pH and has a Q of 18. The Q of the varactors is 8.

The QVCO operates from a 1.5-V supply (lower than the RX's nominal 1.8-V supply voltage), which linearizes the varactors, and hence, helps in achieving a higher tuning range and lower phase noise. This is shown in Fig. 13, where varactor capacitance is plotted as a function of the supply voltage. The average change in capacitance over one oscillation cycle is lower at point A ($V_{DD} = 1.5$ V, where the slope is relatively constant) than at point B ($V_{DD} = 1.8$ V), resulting in a lower phase noise at 1.5-V supply. The measured phase noise at a carrier frequency of 26.5 GHz is -107 dBc/Hz at 1-MHz offset (cf. Section IV), which is better than the phase noise (-104 dBc/Hz) of the SiGe VCO reported in [24]. Note that despite making efforts in lowering the phase noise of the QVCO of Fig. 12, the close-in phase noise of the oscillator will corrupt the extraction of Doppler information from the received signal, and hence, a phase-locked loop (PLL) should be employed. The design of K-band PLLs has been reported in [9], [25], and [26].

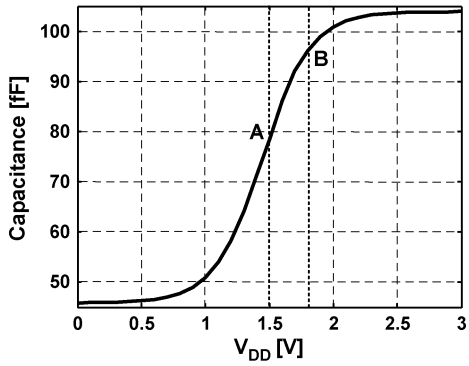


Fig. 13. Varactor capacitance as a function of VCO supply voltage.

The pulse former shown in Fig. 12 is used in each of the I and Q paths to upconvert the BB pulse to the LO frequency. Prior art [27] suggests that the use of 0.18-μm MOS switches in RF transceivers is possible up to frequencies on the order of a few gigahertz only. This limitation exists only for small-signal operation and especially when the switch terminals need to be conjugate-matched to external 50-Ω impedances, e.g., as in a transmit/receive antenna switch. With careful design, MOS switches can be efficiently used in high-frequency large-signal systems, as is demonstrated for the pulse former circuit presented in this study. In fact, the pulse former of Fig. 12 exhibits low on-state insertion loss and superior off-state LO leakage (cf. Section IV).

The design of this pulse former involves several tradeoffs such as: 1) minimizing on-state insertion loss, off-state LO leakage, and rise and fall times; and (2) maximizing dynamic range and pulse energy. In Fig. 12, M_2 and M_5 modulate the differential LO with the BB pulse. The upconverted pulse is

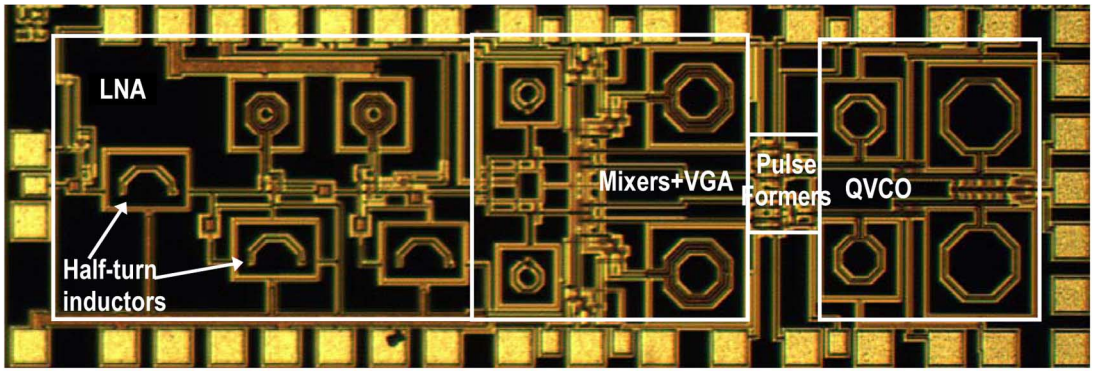


Fig. 14. Die micrograph of the RX front-end measuring 3 mm × 1 mm.

then sent either to the TX or the RX depending on the states of TX-enable (TX_EN) and RX-enable (RX_EN) signals. M_1 serves several important purposes in the pulse former, which are: 1) it acts as a dissipative load for the LO sinusoids when the BB signal is low and 2) it also ensures that a constant impedance is presented to the LO outputs irrespective of the state of the BB pulse. These functions are critical for shielding the LO from switching transients and pulling. While degrading the on-state insertion loss, M_1 improves off-state isolation. 3-V signals are used to enable the switch network so as to minimize on-resistances of the switch transistors. The common mode at the LO port of the pulse former is chosen so as to provide adequate dynamic range while ensuring that the MOS switches operate outside the breakdown region (<2 V between any two MOS terminals for the foundry process used in this study). 1-kΩ resistors (R) are used to improve ac isolation between any two switches driven by the same control signal. Since this study does not include the TX, the differential TX ports of the pulse formers are terminated on-chip by precision 100-Ω resistors. While exhibiting performance comparable to the SiGe design in [28], the I/Q pulse formers in this study occupy a die area of 0.05 mm^2 only and consume zero dc power.

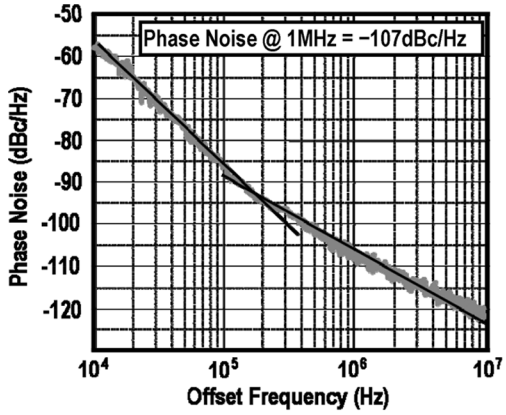
V. Measurement Results

Device modeling, passive component performance, and simulation methodology are major challenges for highly integrated high-frequency designs. In order to alleviate these problems, the RX design was optimized using measured data for active devices and a combination of EM simulations and measurements for passives, as discussed below.

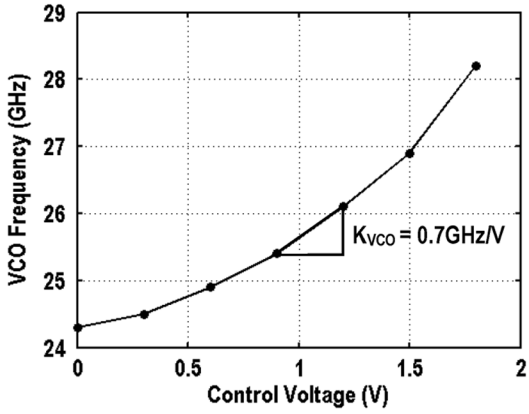
The radar RX front-end was fabricated in a commercial 0.18-μm CMOS process with an NMOS f_T of 55 GHz and six metal layers. Substrate loss and noise coupling severely affect signal integrity at high frequencies, especially in systems with highly sensitive building blocks like VCOs and LNAs. To address these issues, spiral inductors designed in the 2.34-μm-thick top metal layer were surrounded by substrate contacts to reduce substrate noise coupling. Inductors were separated by a minimum distance of 50 μm to minimize both magnetic and electrical coupling. Moreover, the inductors in the I and Q branches in the LO path and the downconversion chain were oriented at 180° to minimize I/Q mismatch. This is especially critical for the QVCO as any stray coupling through the inductors can overshadow the injection-locking mechanism. Half-turn inductors (microstrip) with dedicated return path were designed to realize gate and source-degeneration inductances of 50–100 pH in the LNA. MOS transistors were laid out in a triple well for isolation from substrate noise. Small (70 μm × 50 μm) signal pads were used to reduce pad capacitance, and hence, substrate loss.

Test structures were fabricated for active and passive devices including MOSFETs, MOS varactors, transmission lines, and spiral inductors with corresponding deembedding structures. Measured S-parameter data for active devices was used directly for S-parameter and transient simulations. Parameterized models with optimization capability were developed for inductors and transmission lines using the ADS Momentum EM simulator. These models were used to optimize the initial design of the entire RX front-end. Sonnet EM simulator was calibrated against the measured data from the passive-device test structures. The calibrated Sonnet simulator was then used for further verification and optimization of the passive devices designed with Momentum. Inductors were optimized for low loss and high self-resonance frequency. The microphotograph of the chip is shown in Fig. 14. The chip area is 3 mm × 1 mm including the pads. The dc pads of the chip were wire-bonded directly to a PCB and on-wafer microwave measurements were carried out to characterize the RX performance. The LNA, QVCO, and pulse formers were measured separately. The forward gain S_{21} and NF of the LNA vary from 15.2 to 18 and 4.5 to 6 dB across the 22–29-GHz band. The input return loss S_{11} and reverse isolation S_{12} of the LNA are less than -15 and -35 dB, respectively. Two important parameters were measured for the pulse former. The on-state insertion loss varies from -2.2 dB (at 29 GHz) to -1.5 dB (at 22 GHz). The off-state LO leakage varies from -29.5 dB (at 22 GHz) to -26 dB (at 29 GHz). The QVCO achieves a measured phase noise of -107 dBc/Hz at an offset of 1 MHz from 26.5 GHz, as shown in the phase noise profile in Fig. 15(a). The QVCO frequency is tunable from 24.3 to 28.2 GHz, as indicated in Fig. 15(b).

The measured conversion gain and NF of the RX front-end are shown in Fig. 16. The conversion gain varies from 35 to 38.1 dB and NF is less than 7.5 dB across the entire 22–29-GHz band. NF varies less than 0.5 dB across the VGA gain settings, which is expected because the noise of the BB circuits



(a)



(b)

Fig. 15. (a) Measured phase noise and (b) tuning curve of the QVCO.

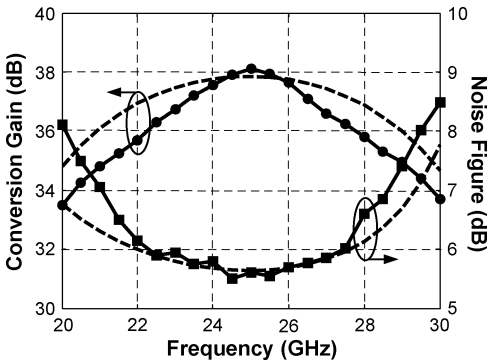


Fig. 16. Measured (solid lines) and simulated (dashed lines) conversion gain and NF of the RX.

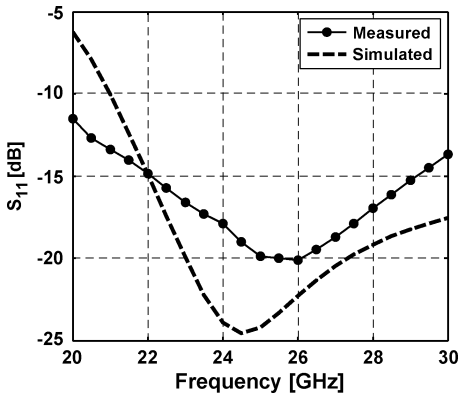


Fig. 17. Measured and simulated input return loss of the front-end.

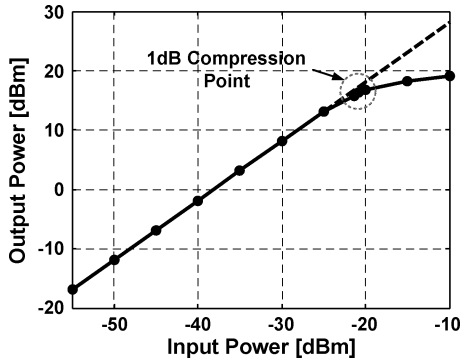


Fig. 18. 1-dB compression point.

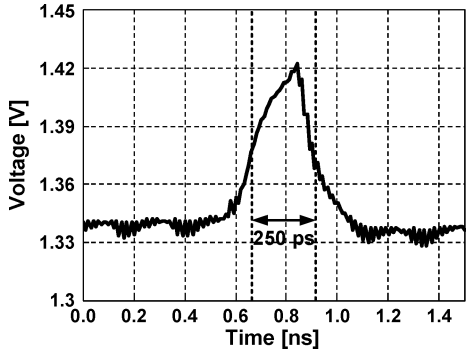


Fig. 19. Measured time-domain pulse output.

TABLE I
COMPARISON WITH RX IN [4]

	This work	RFIC '06 [4]
Integration	LNA + Mixer + VGA + QVCO + Pulse former	LNA + Mixer + VGA + Switch + Integrator
Technology	0.18μm CMOS	SiGe
Bandwidth	21.3-29GHz	22-26GHz (LNA)
Conversion gain	38.1dB	45dB
Noise Figure	5.5dB	7.8dB
Power dissipation	131mW	1.08W

is suppressed by the high LNA gain. The wideband input return loss achieved by the RX is shown in Fig. 17 and is lower than −14.5 dB in the desired band.

On-wafer measurements of the RX chip indicate an input-referred 1-dB compression point $P_{1\,\mathrm{dB}}$ of −20.8 dBm, as illustrated in Fig. 18, and an IIP_3 of −9 dBm. $P_{1\,\mathrm{dB}}$ varies from −20.8 to −13 dBm between the highest and lowest gain settings of the VGA, respectively. Owing to the carefully designed pulse former, the RX achieves excellent port-to-port isolation. The measured LO-to-IF leakage and the LO-to-RF leakage are lower than −23 and −30 dB, respectively, over the entire bandwidth. The measured power consumption of the RX is 131 mW, more than half of which is due to the LO and output buffers.

TABLE II
SUMMARY OF PERFORMANCE

Receiver		**QVCO**	
3dB Bandwidth	21.3-29GHz	Phase Noise @ 26.5GHz	−107dBc/Hz@1MHz
Power Gain	35-38.1dB	Tuning Range	24.3-28.2GHz (14.8%)
Noise Figure	5.5-7.4dB	**Pulse Former**	
Input Return Loss	<−14.5dB	On-state insertion loss	<−2.2dB
Output Return Loss	<−15dB	Off-state LO leakage	<−26dB
IF-to-RF isolation	<−45dB	**Power Dissipation**	
LO-to-RF isolation	<−30dB	LNA	8.3mA @1.8V
LO-to-IF isolation	<−23dB	I/Q Mixer + VGA	20mA @1.8V
1-dB compression point	−20.8dBm	QVCO & Buffers	28mA @1.5V
IIP3	−9dBm	Output buffers	21mA @1.8V
Technology	0.18μm RFCMOS	Total	49.3mA @1.8V 28mA @1.5V
Die Size	3mm^2		

In order to validate the UWB operation of the RX front-end, pulse-based measurements were performed. A narrow-pulse train was applied at the BB ports of the pulse formers, and a 24-GHz sinusoid was fed to the LNA input. The pulse train was upconverted to 24 GHz by the on-chip pulse former and then downconverted to the RX BB after multiplication with the 24-GHz sinusoid from the LNA. The measured transient waveform of the downconverted pulse is shown in Fig. 19. The measured 50% pulsewidth is 250 ps, as shown in Fig. 19.

Table I compares this design with the SiGe RX in [4] designed for the same application. The measured performance of the RX front-end is summarized in Table II.

VI. CONCLUSION

In this paper, we have demonstrated the design of a CMOS UWB RX front-end operating in the 22–29-GHz band suitable for use in automotive short-range radar sensors. On-wafer measurements of the fabricated prototype exhibited excellent results. The front-end achieved a gain of >35 dB and an NF <7.5 dB over the entire UWB 22–29-GHz frequency band, while consuming 131 mW. UWB pulse formation has also been demonstrated. To the authors' knowledge, the RX front-end presented in this study has the best performance reported in 0.18-μm CMOS for short-range automotive radar applications.

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