

Design Issues in Low-Voltage High-Speed Current-Mode Logic Buffers

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Abstract - A current-mode logic (CML) buffer is based on a simple differential circuit. This paper investigates important problems involved in the design of a CML buffer as well as a chain of tapered CML buffers. A new design procedure to systematically design a chain of tapered CML buffers is proposed. The circuit design issues in regard to the CML buffer are compared with those in a conventional CMOS inverter. It is shown, both through the experiments and by using efficient analytical models, why CML buffers are better than CMOS inverters in high-speed low-voltage applications.

1. INTRODUCTION

The rapidly growing volume of data transfer in telecommunication networks has recently drawn considerable attention to the design of high-speed circuits for giga-bit communications networks. Wavelength-division multiplexing (WDM) and time-division multiplexing (TDM) were developed for use in the next-generation transmission systems. Ultra-massive-capacity transmission experiments have been reported using a WDM system with a per-channel data-rates of 10Gbit/sec for SONET OC-192 and 40Gbit/sec for SONET OC-768. High-speed integrated circuit (IC) technologies with very high data-rates are thus required for both WDM and TDM systems. Advances in nanometer CMOS technology has enabled CMOS integrated circuits to take over the territories thus far claimed by GaAs and InP devices.

Designing a high-speed CMOS circuit operating near f_T of the MOS device is very challenging. System blocks in a giga-bit communication system need to be realized by very simple circuits utilizing minimum number of active devices. Parts of the circuit blocks that process high-speed signals in a communication transceiver should possibly abandon to use PMOS devices due to their inferior unity-gain frequency.

Buffers are the circuit core of many high-speed blocks within a communication transceiver and a serial link. As an example of a giga-bit communications system, Fig. 1 depicts the block diagram of a typical optical transceiver. Front-end CML tapered buffer chain, serial-to-parallel converters, clock and data recovery (CDR), multiplexers, and demultiplexers all use high-speed buffers. A conventional CMOS inverter exhibits some drawbacks that prevent it from being vastly used in high-speed low-voltage circuits. First, a CMOS inverter is essentially a single-ended circuit. Recall that in multi-gigahertz frequency range, the short on-chip wires act as coupled transmission lines. The electromagnetic coupling thus causes serious operational malfunctioning in the circuits particularly single-ended circuits. Besides, the PMOS transistor in a static CMOS inverter will severely limit the maximum operating frequency of the circuit [1] [2].

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CMOS current-mode logic buffers were first introduced in [3] to implement a giga-hertz MOS adaptive pipeline technique. The CML circuits can operate with lower signal voltage and higher operating frequency at lower supply voltage than CMOS circuits can. However, CML buffers suffer from dissipating more static power than CMOS inverters. Recently, there have been efforts to alleviate this shortcoming [4]. Due to their superior performance, CML buffers are the best choice for high-speed applications. As a consequence, it is an essential need to have a systematic approach to optimally design CML buffers and CML buffer chains.

This paper presents a comprehensive study of CML buffers and steps that need to be taken to design a chain of tapered CML buffer. The paper is organized as follows. First, in section 2 a brief summary of CMOS inverter is given. Then, in section 3, the large-signal behavior of a differential circuit is extensively illustrated. This will prepare us to study the design of CMOS buffer chain (section 4). Finally, section 5 provides the experimental results that verify the accuracy of our design approach.

2. CMOS BUFFERS

A conventional static CMOS buffer is shown in Fig. 2 (a) where the input-output transfer curve is shown in Fig. 2 (b).

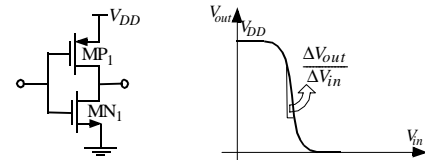


Fig. 2. (a) CMOS inverter. (b) Transfer characteristics

A CMOS inverter has a number of advantages. The static power dissipation of a CMOS inverter is negligible assuming the leakage current to be small. It exhibits the largest small-signal gain compared to any other area-efficient single-stage buffer with the same transistor sizes, and thus is an ideal candidate for bus drivers and signal buffers in digital circuits. It shows an optimum performance with the technology scaling and has a large noise-margin.

A CMOS inverter, however, suffers from a number of drawbacks that make it vulnerable in ultra high-speed integrated circuits. First, use of PMOS transistor degrades the circuit maximum operation frequency (bandwidth). Secondly, like any single-ended circuit, a CMOS inverter is highly susceptible to the environmental noise sources such as power/ground noise and crosstalk. Large current surges during the voltage switching of output CMOS buffers driving large off-chip loads exacerbates the fluctuations on supply and ground rails. Noisy supply and ground wire results in noise-margin reduction as well as a larger propagation delay for all predrivers connected to the same power and ground rail. Shown in Figures 3 (a) and (b), are the input and output voltages and the power/ground bounce noise due to simultaneous switching of 8 CMOS inverters driving a large 2pF off-chip capacitor. Obviously, other CMOS circuits connected to these noisy power and ground rails are affected by large unwanted oscillations that may cause false logic switchings.

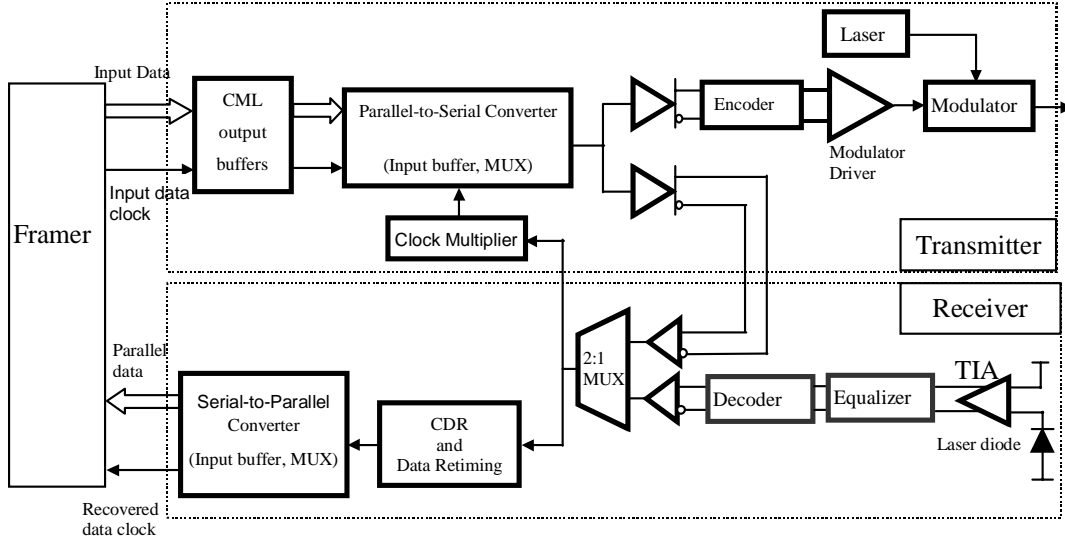


Fig. 1. A system block diagram of an optical transceiver

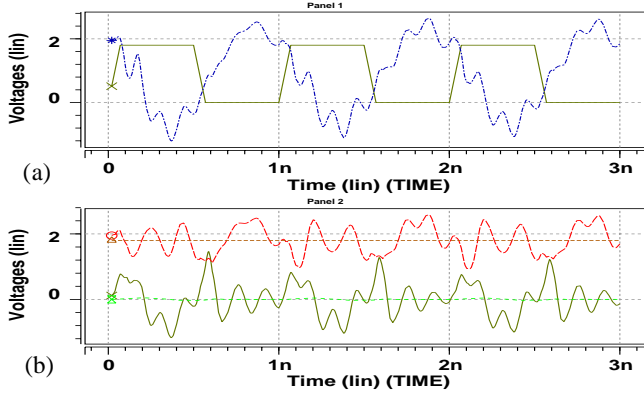


Fig. 3. (a) Input and output voltages of 8 CMOS buffers switching simultaneously. (b) The power/ground bounce

3. CURRENT-MODE LOGIC BUFFERS

A current-mode logic (CML) buffer is based on the differential architecture. Fig. 4. (a) shows a basic differential architecture. The tail current, I_{SS} , provides an input-independent biasing for the circuit. The differential circuit is easily neutralized using a pair of capacitors (Fig. 3(a)), C_D , that will diminish the deleterious effects of input-output coupling through the device overlap capacitance, C_{GD} .

Various experimental simulations of CML circuits reveal that the long-channel transistor model still gives rise to a good estimation of the dynamic behavior of these circuits. The reason is because a CML circuit is a low-voltage circuit where the differential voltage swing is around the device threshold voltage.

As the differential input varies from $-\infty$ to $+\infty$, each output node of the differential pair varies from $V_{DD} - R_D I_{SS}$ to V_{DD} . Fig. 3 (b) shows the voltage variations of the output nodes in terms of the differential input [5].

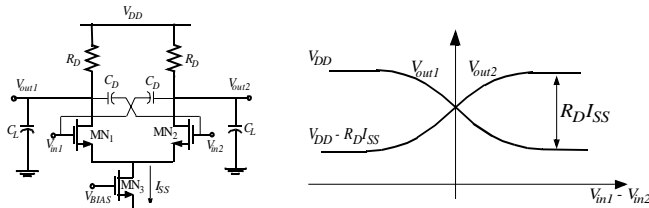


Fig. 4. (a) A neutralized CMOS differential pair. (b) Transfer characteristics.

From Fig. 4. (a) one can see that the maximum output differential voltage swing, V_{odm} , is only a function of the drain resistor and the tail current, provided that the current switching takes place. Clearly, the maximum output swing of a CML buffer is less than that of a CMOS inverter, which makes this class of buffers an ideal choice for low-power integrated circuit design.

The minimum value of the input common-mode level, $V_{in,CM,min}$ is achieved when the tail current begins to operate in saturation. The input common-mode level reaches its maximum value, $V_{in,CM,max}$ when the transistors MN_1 and MN_2 are either at pinch-off or at cutoff [5].

$$V_{GS,12} + (V_{GS3} + V_{THN}) \leq V_{in,CM} \leq \min \left[V_{DD} - R_D \frac{I_{SS}}{2} + V_{THN}, V_{DD} \right] \quad (1)$$

where V_{GS12} is the common-mode overdrive voltage of transistors MN_1 and MN_2 . Similarly, the output common-mode level varies from V_{DD} (when both MN_1 and MN_2 are off, and MN_3 is in the linear region) to $V_{DD} - R_D I_{SS}/2$ (when all transistors are in saturation). The voltage transition of the output common-mode level from V_{DD} to $V_{DD} - R_D I_{SS}/2$ is determined by the subthreshold current of MN_1 or MN_2 .

The advantage of the differential CML buffer is understood by reviewing its large-signal behavior in response to a differential input signal. Assuming that the input common-mode level is bounded within the operating range specified in Eq. (1), a small voltage difference between V_{in1} and V_{in2} results in a corresponding differential current $I_{D1} - I_{D2}$, as follows [5]:

$$\Delta I_D = I_{D1} - I_{D2} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \Delta V_{in} \sqrt{\frac{4I_{SS}}{\mu_n C_{ox} \frac{W}{L}} - \Delta V_{in}^2} \quad (2)$$

The differential current is an odd function of the input differential voltage, ΔV_{in} , and thus becomes zero when the circuit is in equilibrium. Furthermore, a differential stage is more linear than a single-ended stage due to the absence of the even harmonics from the input-output characteristics. The large-signal transconductance, G_m , is the slope of $\Delta I_D - \Delta V_{in}$ transfer characteristics, that is:

$$G_m = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \frac{2\Delta V_{in,max}^2 - 2\Delta V_{in}^2}{\sqrt{2\Delta V_{in,max}^2 - \Delta V_{in}^2}} \quad (3)$$

where $\Delta V_{in,max} = \sqrt{2I_{SS} / (\mu_n C_{ox} \frac{W}{L})}$. The large-signal transconductance varies with the input differential voltage, as also shown in Fig. 5, where in this figure $\Delta V_{in,max} = 0.4$ V. As the input differential voltage exceeds a limit, one transistor carries the entire cur-

rent, I_{SS} , turning off the other transistor. $\Delta V_{in,max}$ represents the maximum input differential voltage.

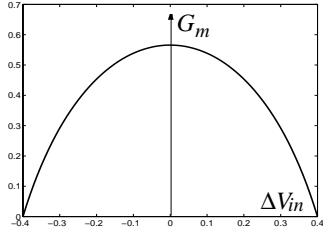


Fig. 5. Large-signal G_m as a function of the differential input

An input-dependent transconductance results in a nonlinear large-signal gain. To simplify the analysis the average value of the transconductance is utilized.

$$G_{m,avg} = \frac{\int_0^{\Delta V_{in,max}} G_m(\Delta V_{in}) d(\Delta V_{in})}{\int_0^{\Delta V_{in,max}} d(\Delta V_{in})} = \sqrt{\frac{1}{2} \mu_n C_{ox} \frac{W}{L} I_{SS}} \quad (4)$$

A differential pair architecture using a differential signaling is insensitive to common-mode fluctuations, which makes it a better choice as a buffer than a CMOS inverter, particularly in low-noise circuit design where noise mostly appears as a common-mode component. Moreover, a non-inverting buffer is easily realized using a single differential stage, as opposed to the CMOS inverter where a non-inverting buffer is realized by two inverters in cascade. Therefore, a non-inverting differential buffer exhibits a lower propagation delay than a CMOS buffer. A differential stage will be operating as a CML buffer iff a complete current switching takes place. To make sure that the current switches entirely from one side of the differential stage to the other side, the differential input voltage must be at least $\Delta V_{in,max}$.

4. TAPERED CML BUFFER DESIGN

To achieve the best performance in a CML buffer, a complete current switching must take place, and the current produced by the tail current needs to flow through the ON branch only. In a tapered buffer chain a CML buffer drives another buffer, which means that output terminals of the driving buffer stage are connected to the input terminals of the driven stage, as shown in Fig. 6. To satisfy the above performance requirement, the differential voltage swing of the first CML buffer must exceed $\Delta V_{in2,max}$ of the following stage:

$$R_{D1} I_{SS1} \geq \sqrt{2 I_{SS2} \left(\mu_n C_{ox} \left(\frac{W}{L} \right)_2 \right)} \quad (5)$$

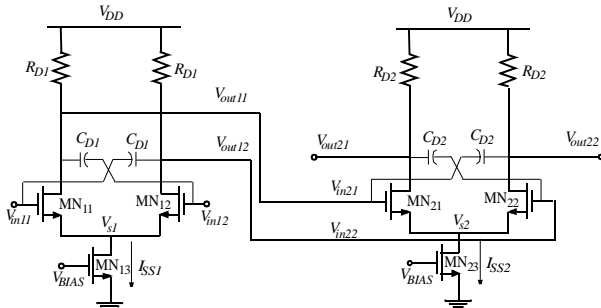


Fig. 6. Two CML buffers in cascade

Furthermore, the load resistors should be small in order to reduce the RC delay and increase the bandwidth. To guarantee a high-speed operation, NMOS transistors of the differential pair must operate only in the saturation. To satisfy this requirement for the

circuit shown in Fig. 6, first, the input common-mode voltage must be within the interval specified in Eq. (1); and secondly,

$$V_{in_k,max} - V_{THN} \leq V_{out,kj} \leq V_{DD} \quad \text{for } k=1,2 \text{ and } j=1,2 \quad (6)$$

which sets a maximum allowable level for the differential output swing as follows:

$$R_{Dk} I_{SSk} \leq V_{THN} \quad \text{for } k=1,2 \quad (7)$$

In addition, a high-speed CML output driver must drive a large off-chip load through the bondwire and package trace. The output driver must thus have a large current drive capability. This means that NMOS transistors of the second CML buffer in Fig. 6 must be large. A large transistor has a large gate-to-channel capacitance that seriously degrades the propagation delay and the voltage swing of the preceding predriver stage. To reduce the propagation delay of the predriver, a chain of tapered buffers is introduced between the first predriver stage and the second buffer. The minimum delay is obtained by dividing the delay equally over all stages. This is achieved by gradually scaling up all stages with a constant taper factor, u . On the other hand, the chip package interface at very high frequencies is appropriately modeled as a transmission line that is terminated by a load impedance, which is a series RC circuit (*cf.* Fig. 7). The series load resistance, Z_0 , provides the high-frequency parallel matched termination to the bondwire. Fig. 7 shows the schematic of the output CML driver driven by $N-1$ tapered CML buffers along with the chip-package interface being modeled as the transmission line.

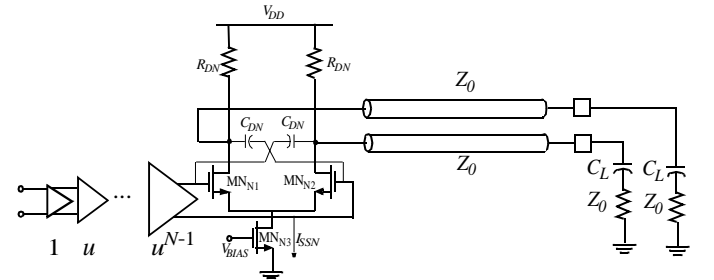


Fig. 7. An output CML buffer driving off-chip loads. The chip-package interface is electrically modeled using a lossless transmission line.

The chip bondwires exhibit high-Q inductances. Therefore it is safe to model the chip-package interface using a lossless transmission line. To avoid potentially disastrous transmission line effects such as slow ringing and propagation delays, the bondwires are terminated both at the source using a series termination ($R_{DN} = Z_0$), and at the destination using a parallel termination (Z_0). Given a well-defined output voltage swing ($R_D I_{SS}$) and with R_D being determined by the matched termination, the tail current I_{SSN} is easily calculated. For instance, an output differential voltage swing of 0.4V for a 50Ω line driver requires a bias current of 8mA. Now, using a set of constraints, we present design guidelines to design a tapered CML buffer chain and determine appropriate values for the circuit components of the CML buffer.

The propagation delay is computed using the open-circuit time constant method [6]. For instance, the delay of the simple low-voltage differential stage of Fig. 3 is $0.69 R_D C_L$. Various HSPICE simulations on high-speed CML buffers show that the delay obtained by the open-circuit time-constant method is within 8% of the actual simulation.

Minimizing the overall propagation delay of CML buffer increases the overall operation frequency of the buffer significantly. For a slowly varying input signal, increasing the small-signal voltage gain will further decrease the output transient variations and the output transition time. In a chain of tapered CML buffers, to attain a constant voltage swing, transistor sizes are scaled up while the drain resistances are scaled down with a constant scaling factor.

This will lead us to the fact that small-signal voltage gains of all constituting stages of the buffer chain are identical.

As a consequence, Eq. (5) provides us with a lower bound for the maximum small-signal voltage gain at equilibrium, that is:

$$\left(A_{v,eq} = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS} R_D} \right) \geq \sqrt{2} \quad (8)$$

The drain resistor, R_{DN} , of the last output CML buffer is determined by the series impedance matching to bondwire's characteristic impedance. Subsequently, I_{SSN} of the last driver stage is calculated using the output differential voltage swing and R_D . The only remaining parameter in the last CML driver left is the (W/L) of the source-coupled transistor pair, which is obtained from the common-mode characteristic of the last CML buffer. If the common-mode input voltage lies in the allowable range given by Eq. (1), then the tail current is equally divided between the two branches of the differential stage, i.e.,

$$(V_{in_k,CM} - V_{sk} - V_{THN} \geq V_{in_k,CM} - V_{BIAS} - 2V_{THN}) = \sqrt{I_{SSk} / \left(\mu_n C_{ox} \left(\frac{W}{L} \right)_k \right)} \quad \text{for } k = 1, 2, \dots, N \quad (9)$$

where $V_{in_k,CM}$ is the common-mode input voltage of the k^{th} driver in the buffer chain. $V_{in_k,CM}$ is specified by the output common-mode voltage of the previous stage. Given a **tapered buffer chain** with a constant differential voltage swing, the maximum (W/L) of the transistor pair of the k^{th} CML buffer is then calculated by solving Eq. (10):

$$V_{DD} - R_D \frac{I_{SS}}{2} - V_{BIAS} - 2V_{THN} = \sqrt{I_{SSk} / \left(\mu_n C_{ox} \left(\frac{W}{L} \right)_k \right)} \quad (10)$$

In the above equation $R_D I_{SS}$ is the constant differential output swing of a tapered CML buffer chain.

As mentioned above, in a chain of tapered CML buffers, the minimum delay is obtained by dividing the delay equally over all stages. However, the question is how many buffer stages are required to achieve the optimum delay. To answer this question, the propagation delay of an arbitrarily chosen CML stage in a buffer chain is first derived. Fig. 8 shows the k^{th} stage in a chain of N tapered stages driving another CML stage along with the capacitors that contribute to the delay calculation.

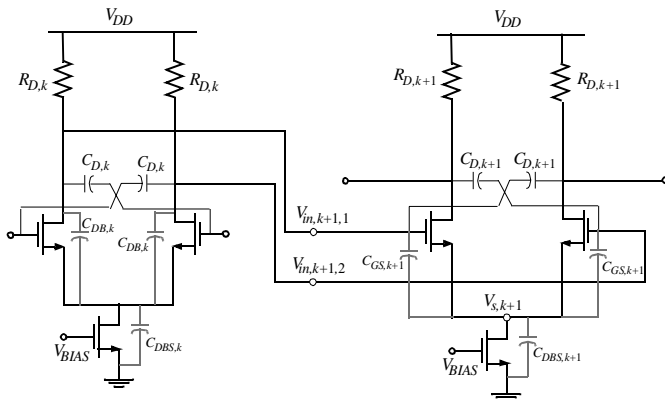


Fig. 8. The k^{th} and $(k+1)^{\text{st}}$ stages of a tapered CML buffer along with the parasitic capacitances

The common node s_{k+1} shown in Fig. 8 undergoes a smaller variation compared to the voltage variations of the input terminals particularly in a matched differential pair. In fact, it is easily shown that for a maximum differential input variation of $\Delta V_{in,max}$ derived in Section 3, the maximum variation of the common node is

$\Delta V_{in,max} / \sqrt{2}$. Therefore, the equivalent capacitance seen at the common node s_{k+1} is approximately $C_{s,k+1} = \sqrt{2} C_{DBS,k+1}$ rather than $C_{DBS,k+1}$.

The 50% delay of the k^{th} stage is as follows:

$$t_{d,k} = 0.69 R_{D,k} (C_{DB,k} \textcircled{S} C_{s,k} + C_{GS,k+1} \textcircled{S} C_{s,k+1}) \quad (11)$$

where \textcircled{S} represents the series connection of electrical elements. The total propagation delay of the buffer chain is readily calculated:

$$t_d = \sum_{k=1}^N t_{d,k} = 0.69 N R_{D1} (C_{DB1} \textcircled{S} C_{s1} + X^{1/N} C_{GS1} \textcircled{S} C_{s1}) \quad (12)$$

Interestingly, the functional dependence between delay and the number of stages (or taper factor) is similar to the one in a CMOS buffer chain [7]. To be more specific, consider a chain of tapered CML buffers driving a lossless transmission line with a characteristic impedance of Z_0 . Suppose that the gate aspect-ratio of the transistor pair of the last CML line driver is X times larger than that of the first predriver stage. It is easily proved that if $C_{DB1} = \gamma C_{s1}$ and $C_{GS1} = \eta C_{s1}$; then it is easily proved that the optimum number of stages will be the numerical solution to the following equation:

$$X^{1/N_{opt}} = \exp \left[\frac{\frac{\gamma/\eta}{1+\gamma} + \left(\frac{1}{1+\eta} \right) X^{1/N_{opt}}}{\left(\frac{1}{1+\eta} \right) X^{1/N_{opt}}} \right] \quad (13)$$

or in the special case, if $C_{DB1} \ll C_{GS1}$ then, $N_{opt} = \ln(X)$ which is well-known result.

To further increase the bandwidth (reduce the delay), the intermediate stages use inductive peaking as demonstrated in Fig. 9. The inductive peaking proves extremely useful to enhance the performance of ultra high-speed circuits operating at frequencies greater than 5GHz.

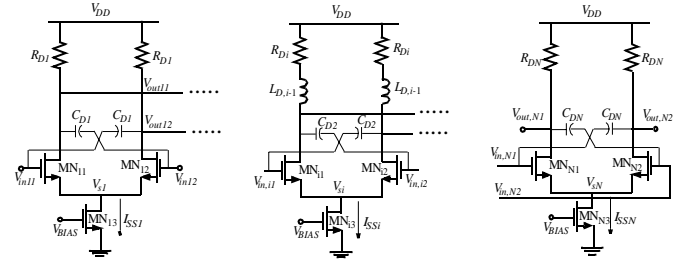


Fig. 9. Multiple stage CML buffers along with the inductive peaking

The addition of the inductor in series with the drain resistor delays the current flow through the branch containing the resistor, making more current available for charging the device capacitors, and reducing the rise and fall times. Inductive peaking can increase the bandwidth to about 1.72 times larger than the unpeaked case [6]. Inductance values are scaled with the same taper factor as the drain resistors are.

5. SIMULATION RESULTS

In this section the performance of the CML buffer is evaluated by performing experiments on single stage as well as multiple stages of the buffer. First, the noise susceptibility of the CML buffer is experimentally compared with CMOS inverter. Next, the accuracy of Eq. (13) is verified by running HSPICE simulation on a chain of CML buffers. Finally, the effect of inductive peaking on the bandwidth and speed enhancement will be investigated.

5.1. Noise Performance

A CML buffer exhibits a superior noise performance compared to a conventional CMOS inverter, particularly because environmental noise sources (e.g., crosstalk) appear as common-mode signals. This will be experimentally verified by performing the following experiment.

First, crosstalk noise is emulated using parallel interconnects located within close proximity of each other, as depicted in figures 10 (a) and (b).

To have a performance comparison, we place, first, a CMOS inverter, and then, a CML buffer at the outputs of coupled interconnects, one at a time (figures 10 (a) and (b)). To highlight the superiority of noise performance of the CML buffer, the middle line in Fig. 10 (b) will be driven by a CMOS inverter. The noise amplitude coupled from this line to its neighboring lines is, therefore, excessively large. The input signal frequency for all CMOS inverters is 3.3GHz, while it is 3.5GHz for CML buffers. As a consequence, this experiment also shows the performance of CML buffer in the presence of harmonic distortion. All circuits are designed using 0.18 μ m standard MOS process.

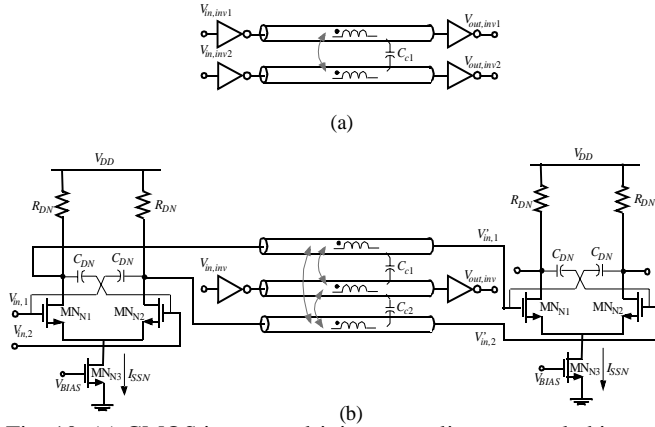


Fig. 10. (a) CMOS inverters driving two adjacent coupled interconnects that are terminated by CMOS inverters. (b) Two interconnects driven by a CML buffer and coupled to another interconnect which is driven by CMOS inverter.

Figures 11 (a) and (b) demonstrate the output signals of CMOS inverter and CML buffer, respectively. The experiment is set up to demonstrate the worst-case scenario in which the noise fluctuation and the voltage waveform are 80° out of phase.

The output voltage $V_{out,inv}$ of the CMOS inverter in Fig. 11 (b) does not have a rail-to-rail swing because of the crosstalk noise effect from the other adjacent line. In fact, this CMOS inverter is incapable of generating a logic "LOW". On the other hand, the functionality of a CML buffer remains intact in the presence of the coupling noise from a neighboring line, as seen in Fig. 11(b).

5.2. Tapered CML buffer experiment

Similar to a CMOS tapered buffer, a single CML buffer might not be sufficient to drive an off-chip load. There are, however, more design trade-offs involved in the design of a CML tapered buffer than in a CMOS tapered buffer. A superior high-frequency performance in a CML buffer is guaranteed only if the design guidelines explained thoroughly in Section 4 to be taken into consideration.

Fig. 12 (a) plots propagation delay as a function of number of CML stages for different values of X, where X is the ratio between the off-chip load impedance and the load impedance of the first pre-driver stage. In practice, X is between 30-100. The optimum number of buffer stages will thus be between 3-4. Fig. 12 (b) depicts the delay vs. number of stages for tapered CMOS buffer. The delay variation in terms of the number of stages for CML tapered buffer and CMOS tapered buffer are almost identical. However, the total propagation delay of a CML buffer chain for a given value of X is less than that of CMOS buffer chain, which is in accordance with what is expected. Remember that 50% propagation delay of a CMOS inverter is inversely proportional to NMOS and PMOS transconductance parameters and directly proportional to the load capacitance [1]. According to (11), the propagation delay of a CML

buffer is directly proportional to the load capacitance (similar to a CMOS inverter) and the drain resistance. A larger threshold voltage and a lower drift velocity associated with a PMOS transistor cause the propagation delay of a CMOS inverter to be larger than that of a CML buffer that uses the same transistor size (Figures 12 (a) and (b)).

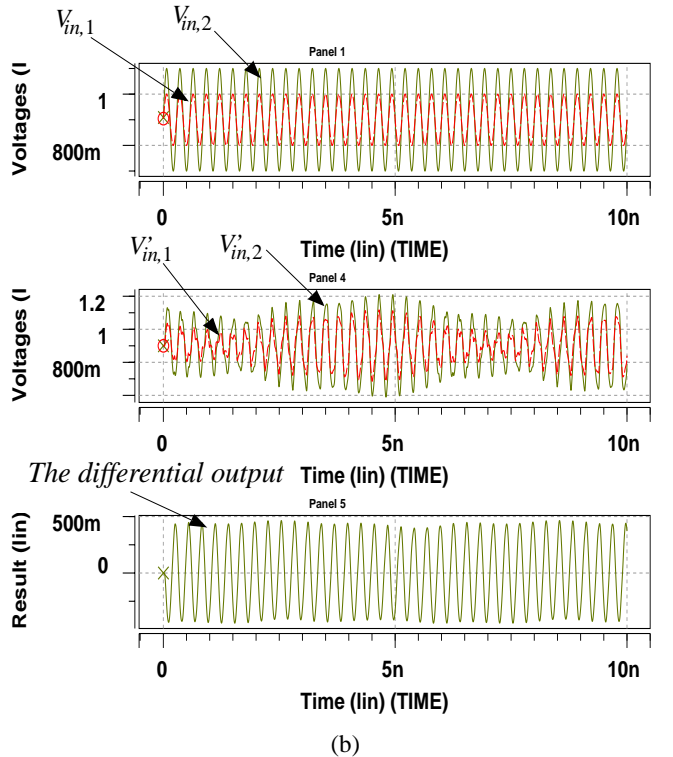
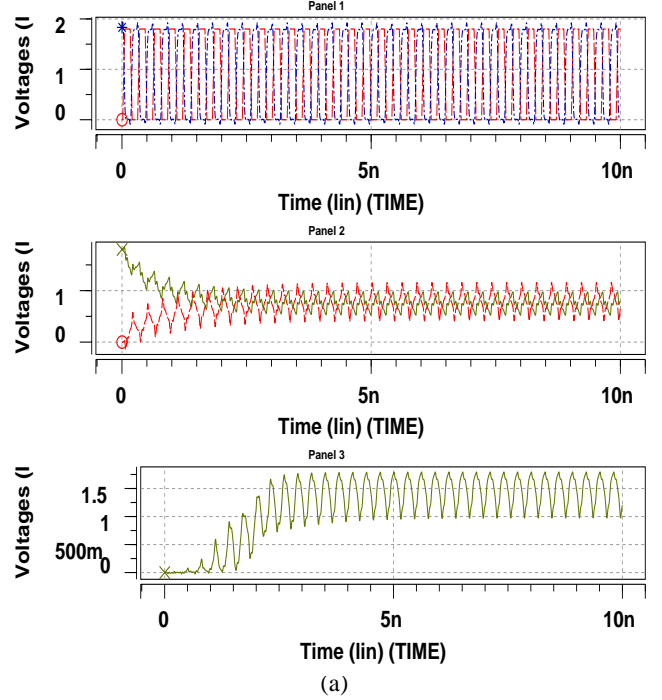


Fig. 11. (a) Input and output waveforms of Fig. 10 (a). (b) Input and output signals of Fig. 10 (b).

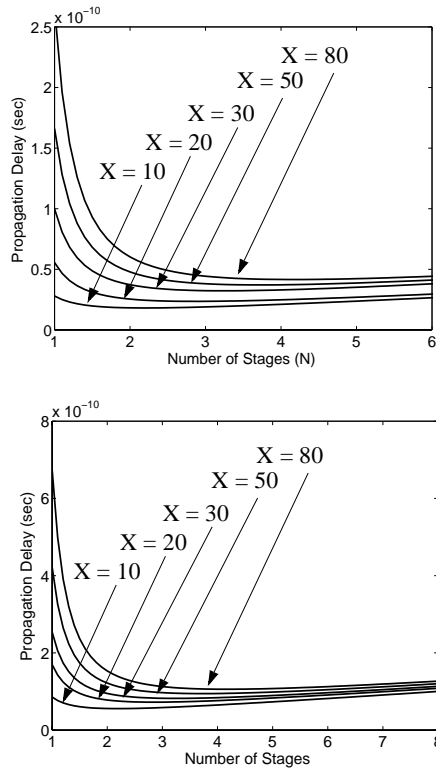


Fig. 12. (a) Delay vs. number of stages for CML tapered buffer chain. (b) Delay vs. number of stages for CMOS tapered buffer chain.

5.3. Inductive peaking

The inductive peaking was proposed as an efficient and simple circuit technique to speed up the buffer's response. Figures 13 (a) and (b) demonstrate the differential output voltage of a CML buffer without and with the inductive peaking, respectively. The inductance value is 4nH and signals are running at 5GHz which is the frequency set forth in SONER/SDH OC-48. The output voltages of CML buffer in the presence of inductance will have larger amplitude and as a result faster rise and fall times.

6. CONCLUSIONS

In this paper we presented the important problems involved in the design of a CML buffer as well as a chain of tapered buffers. We proposed a new design procedure to systematically design a chain of tapered CML buffers is proposed. The circuit design issues in regard to the CML buffer were compared with those in a conventional CMOS inverter. It was also shown, both through the experiments and by using efficient analytical models, why CML buffers are better than CMOS inverters in high-speed low-voltage applications. Experimental results demonstrate the accuracy of the analytical predictions compared to the measured results.

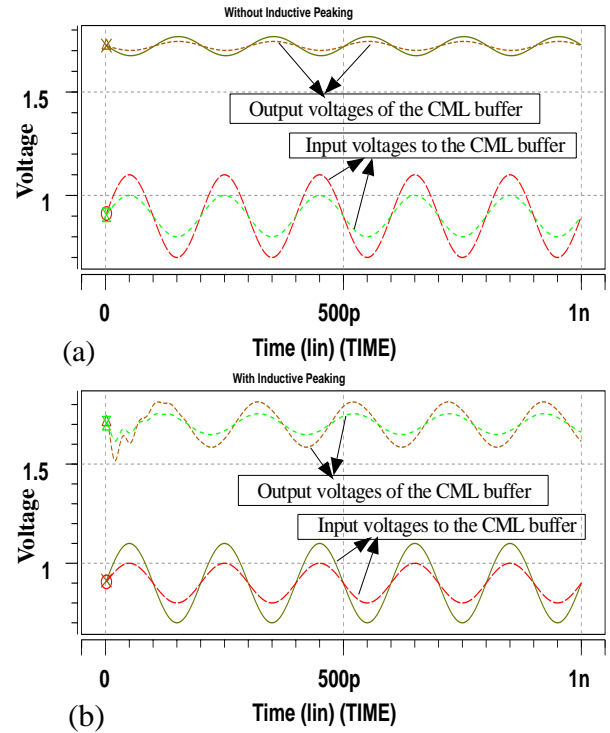


Fig. 13. (a) Input and output waveforms of a CML buffer without inductive peaking. (b) Input and output waveforms of a CML buffer with inductive peaking.

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