# A Novel Linearization Technique for Linear/Pseudo-Linear RF CMOS Power Amplifiers

Ying Zhang and Payam Heydari Department of Electrical and Computer Engineering University of California, Irvine, USA E-mail: {yzhang3, pheydari}@uci.edu

Abstract—A novel linearization technique for linear and pseudo-linear CMOS power amplifiers (PAs) is presented. The proposed technique uses the third-order harmonic of the PA output to generate a signal, which compensates the nonlinear component at the fundamental frequency of the PA output. The reconstructed signal is then subtracted from the output of the PA to cancel out its nonlinear component. A class-AB CMOS power amplifier incorporating this technique is designed and fabricated in a standard 0.18µm CMOS process. Experimental results of this class-AB PA at 900MHz are presented. A twotone test with frequency spacing of 1MHz shows a 12-dB reduction of the IMD3 component.

## **1. INTRODUCTION**

The design of a power amplifier (PA) used in a wireless communication transceiver entails satisfying various design objectives, such as power-added efficiency, total harmonic distortion (THD), and current capability. In modern digital mobile communication systems, linear modulation schemes such as QPSK and multi-level QAM are widely adopted to improve spectral efficiency and system capacity. However, modulated signals obtained using these schemes have fluctuating envelopes which cause spectral regrowth as well as intermodulation distortion (IMD) when amplified through a nonlinear power amplifier. Consequently, linear/pseudo-linear RF power amplifiers are required for wireless communication systems which use QPSK and multi-level QAM modulation techniques.

Many linearization techniques for PAs have been developed to overcome these problems. Predistortion [1], [2], feedback [3], [4], and feedforward [5], [6] are the most commonly used linearization techniques.

In the digital predistortion technique proposed in [1] and [2], the baseband signal is first converted to a digital signal using an A/D converter. The digital signal is then fed to a processor providing sample-by-sample predistortion, and finally converted back to the analog domain prior to modulation and power amplification. This technique offers good IMD suppression. However, its application is limited due to the tradeoff between high-level complexity of this technique and performance. Feedback technique proposed in [3] and [4] exhibits a lower complexity, while offering reasonable IMD suppression. However, the stability considerations inherent in any feedback system limit its application in radio frequencies. Feedforward linearization [5], [6] does not suffer from stability problem and gives good IMD suppression. A major drawback of the feedforward technique is high complexity, which in turn leads to high cost and sensitivity to the environmental variations (e.g., temperature and process variations).

Recently, a variety of simple approaches for the PA linearization have been proposed. A linearization method using interstage second harmonic enhancement has been proposed in [7]. Nevertheless, this technique can only be used in two-stage power amplifiers. In addition, it is hard to tune the parameters of the circuits employed in the linearizer to set the nonlinearity of the PA to zero. In a transistor-level linearization proposed in [8], the positive thirdorder harmonic of I-V relationship in the PMOS device is employed to cancel the negative third-order harmonic of the NMOS I-V relation. Obviously, the nonlinearity cannot be totally canceled out due to the fact that PMOS and NMOS I-V relations are not identically matched across the whole voltage range at the PA input. Furthermore, this technique is technology-dependent.

In this paper, we propose a novel linearization technique, which exploits the third-order harmonic of the PA output to generate a signal, which is exactly equal to the nonlinear component at the fundamental frequency of the PA output. This signal is then subtracted from the output of the PA to cancel its nonlinearity component. A class-AB CMOS power amplifier employing the proposed linearization technique is designed and fabricated in a standard 0.18µm CMOS process. The principle of the proposed technique is described and experimental results of the AM-AM distortion of the class-AB power amplifier at 900MHz are presented. A two-tone test with frequency spacing of 1MHz shows a maximum IMD3 reduction of 12dB.

The remaining part of this paper is organized as follows: Section 2 gives an overview of the nonlinearity effects in a large-signal PA circuit. The underlying principle of the proposed linearization technique is also introduced in Section 2. Section 3 provides the circuit realization of the PA circuit as well as the proposed feedforward technique. Section 4 provides the experimental results. Finally, Section 5 presents conclusions of our paper.

## 2. PRINCIPLE OF THE PROPOSED LINEARIZATION TECHNIQUE

#### 2.1. An overview of the nonlinearity effects

The comprehensive knowledge about the linear system behavior supported by many useful theories makes the linear model a useful approach to study the analog and RF circuits. Nonetheless, nonlinearities often lead to important phenomena that cannot be explained or analyzed using the linear model. This is particularly conceded in regard to a power amplifier, which is the last stage of a RF transmitter prior to the antenna, as depicted in Fig. 1. As a consequence, the incoming signal is indeed a large signal, thereby necessitating a circuit model that accounts for the PA nonlinearities.

In fact, the input and output relationship of the PA using the Laurent series is given in Eq. (1). Since the storage elements in the constituent tank circuit (i.e., inductors and capacitors) resonate out each other at the center frequency, the PA will be appropriately

modeled as a memoryless system<sup>1</sup>:

$$V_{out} = c_1 V_{in} + c_2 V_{in}^2 + c_3 V_{in}^3 + \sum_{k=4}^{\infty} c_k V_{in}^k$$
(1)



Figure 1. A simplified block diagram of the RF front-end of a wireless transceiver

The higher order terms in Eq. (1) for  $k \ge 4$  are negligibly small in an electronic circuit compared to the first three harmonics [9]. The underlying idea of the proposed linearization technique is understood by applying a single-carrier input signal, represented by a sine wave,  $V_{in} = V_{im} \cos \omega_{in} t$ , to the input,

$$V_{out} \approx c_{1}V_{in} + c_{2}V_{in}^{2} + c_{3}V_{in}^{3}$$

$$= c_{1}V_{im}\cos\omega_{in}t + c_{2}(V_{im}\cos\omega_{in}t)^{2} + c_{3}(V_{im}\cos\omega_{in}t)^{3}$$

$$= c_{1}V_{im}\cos\omega_{in}t + c_{2}V_{im}^{2}(\frac{1+\cos2\omega_{in}t}{2}) + c_{3}V_{im}^{3}(\frac{3\cos\omega_{in}t + \cos3\omega_{in}t}{4})$$

$$= \frac{1}{2}c_{2}V_{im}^{2} + \underbrace{(c_{1}V_{im} + \frac{3}{4}c_{3}V_{im}^{3})\cos\omega_{in}t}_{Fundamental component} + \frac{1}{2}c_{2}V_{im}^{2}\cos2\omega_{in}t + \frac{1}{4}c_{3}V_{im}^{3}\cos3\omega_{in}t$$
(2)

The simple input-output relationship in Eq. (2) reveals an important phenomenon in a nonlinear system including a PA circuit, that is, the fundamental frequency component of the output signal constitutes two terms: (1) the first term,  $c_1 V_{im} \cos \omega_{in} t$ , whose amplitude is linearly proportional to the input amplitude with a gain of  $c_1$ , and (2) the second term,  $(3/4)c_3 V_{im}^3 \cos \omega_{in} t$ , whose amplitude is proportional to  $V_{im}^3$  with a gain of  $c_3$ , which is the third-order coefficient in the input-output relationship of a nonlinear system. The gain of the PA is defined as the amplitude of the fundamental component of the output to that of the input. It has been proven that in a CMOS power amplifier  $c_3 < 0$ , when the MOS transistor of the PA operates in the saturation region [10]. Therefore, the PA gain decreases with large input amplitudes, as also demonstrated in Figure 2. This phenomenon is what is commonly referred to as the gain compression. The gain approaches to zero for sufficiently high input levels.

Another criterion to study the nonlinear behavior of the PA is "intermodulation distortion (IMD)", which is measured using the well-known "two tone test" as shown in Figure 3.

The intermodulation components at  $2\omega_1-\omega_2$  and  $2\omega_2-\omega_1$  will result in troublesome effects in RF circuits. If the difference between  $\omega_1$  and  $\omega_2$  is small, these components will fall in the band of interest and corrupt the fundamental frequency component.



Figure 3. Intermodulation in a nonlinear PA

 $(\Omega_1,\Omega_2)$ 

 $2\omega_1 - \omega_2 \quad 2\omega_2 - \omega_1$ 

#### 2.2. The proposed linearization technique

 $\omega_1 \ \omega_2$ 

As explained in the foregoing section, the power amplifier exhibits gain compression at higher level input amplitudes due to the presence of the term  $3/4c_3V_{im}^3$ , simply referred to as nonlinear term, which is added to the linear component of the gain,  $c_1V_{im}$ . The idea for the linearization is thus very simple. To linearize the power amplifier, the nonlinear component,  $(3/4)c_3V_{im}^3$ , must be canceled out. However, this nonlinear component is proportional to  $c_3$ , which is the third-order coefficient of the nonlinear input-output relationship. Noticing that the amplitude of the third-order harmonic in Eq. (2) is also proportional to  $c_3$ , we utilize the third-order harmonic of the output to synthesize a signal at the fundamental frequency with the same amplitude as the nonlinear term of the PA output. The proposed linearization technique is thus carried out in three steps:

- 1. Extract the third-order harmonic using a band-pass filter with a center frequency at  $3\omega_{in}$ .
- 2. Downconvert the third-order harmonic to the fundamental frequency  $\omega_{in}$  using a downconversion mixer
- 3. Subtract the synthesized signal from the PA output.

The mixer must downconvert  $3\omega_{in}$  to  $\omega_{in}$  with a conversion gain of 3 (9.5dB). The block diagram of the proposed linearization technique is shown in Figure 4.



Figure 4. Block diagram representation of the proposed linearization technique

According to Figure 4, the input signal running at frequency  $\omega_{in}$  is amplified by the power amplifier, which introduces harmonics. A band-pass filter (BPF), whose center frequency is at  $3\omega_{in}$ , filters the third harmonic of the output. The filter output is then transferred to the input of a mixer. The downconversion mixer downconverts the  $3\omega_{in}$  frequency component to  $\omega_{in}$  by mixing it with a tone signal at  $2\omega_{in}$ . As mentioned above, a conversion gain of 3 (9.54 dB) is

<sup>&</sup>lt;sup>1</sup> Clearly, a more accurate transient analysis should include the impact of the storage elements, which manifests itself in a nonlinear differential equation for the input-output relationship.

required to fully reconstruct the signal with amplitude of  $(3/4)c_3V_{im}^3$  from the  $3^{rd}$  order harmonic with amplitude of  $(1/4)c_3V_{im}^3$ . Using the BPF and the mixer, a signal at the input fundamental frequency is thus generated that has the same amplitude as the nonlinear fundamental term at the PA output. This signal is finally subtracted from the PA output, thereby canceling the nonlinearity from the power amplifier.

## **3. CIRCUIT IMPLEMENTATION**

A class-AB CMOS power amplifier is designed and implemented to verify the proposed linearization technique. The schematic of PA is shown in Figure 5. This PA delivers a 26-dBm output power to a 50- $\Omega$  load at 900 MHz from a 1.8-V supply voltage. Figure 6 demonstrates the schematic of the 3<sup>rd</sup>-order LC circuit employed in this work to realize a Butterworth band-pass filter. The values for the shunt and series element are given in Table 1. In order to achieve the conversion gain, an active mixer is required which exhibits lower noise figure (NF) [11], and demands smaller LO power compared with its passive counterpart. A double-balanced Gilbert cell, shown in Figure 7, is employed as the downconversion mixer in the design. On-chip square spiral inductors are used to design all constituent inductors. As a design consideration, inductors used in the Gilbert-cell mixer must exhibit a high Qfactor to cancel the harmonics.



Figure 5. Class-AB power amplifier



Figure 7. Double-balanced Gilbert cell mixer

Table 1. Values for the passive elements used in the filter of Figure 6

$L_1(nH)$	$C_1(pF)$	L <sub>2</sub> (nH)	C <sub>2</sub> (fF)	L <sub>3</sub> (nH)	C <sub>3</sub> (pF)
0.88	3.96	20	173	0.88	3.96

As illustrated in Section 2.2, the conversion gain of the mixer should be 9.5dB. However, a conversion gain of 15dB is required in the actual design in order to compensate for the power loss of the constituent passive filter. The waveforms and spectra of the inputs and output of the Gilbert cell mixer are shown in Figure 8, where the output of the BPF is given to the RF terminal. Clearly, in the proposed system in Figure 4, the output of the subtractor is the

actual provider of the signal power to the antenna. It is indeed impossible to design an active subtractor which has enough driving capability to drive the antenna load. As a consequence, a transformer is used as a passive subtractor to achieve sufficient driving capability. The transformer utilized to subtract high power signals is bulky. An off-chip transformer is thus employed to realize the subtraction.



Figure 8. Input and output waveforms and spectra of the mixer

### 4. EXPERIMENTAL RESULTS

In order to verify the proposed technique, a class-AB CMOS power amplifier with the proposed linearization technique is designed and implemented.

Results of the single-tone test at 900MHz for the PA with and without the linearization are shown in Figures 9 and 10. As shown in Figure 9, the input-output power transfer curve of the PA circuit using the proposed linearization circuit is very close to a straight line when the input varies from -20dBm to 4dBm. As explicitly shown in Figure 10, the linearization technique is very effective in improving the gain compression. The gain compression of the PA with linearization is 4.5 dB better than that without linearization at an input power of 2 dBm. Consequently, the 1-dB compression point moves up to higher input levels (i.e., constant power gain for wider range of input power).



Figure 9. Output power of the PA with and without linearization vs. Input power



Figure 10. Power gain of the PA with and without linearization vs. Input power



Figure 11. Spectrum of the PA without linearization



Figure 12. Spectrum of the PA with linearization

A two-tone test centering at 900 MHz with frequency spacing of 1 MHz is carried out for the power amplifier. Figures 11 and 12 shows the frequency spectrums of the PA with and without the proposed linearization, respectively, and when the output power is 23dBm. As depicted in Figure 11, the IMD of the PA without linearization is -17dBc. The IMD of the PA is greatly reduced using the linearization technique, as also shown in Figure 12. More precisely, using the proposed linearization technique, the IMD3 is reduced to -29dBc, hence a 12-dB improvement in the circuit linearity. Figure 13 shows the IMD3 of the PA with and without the proposed linearization, when the output power varies from 12dBm to 26dBm. A maximum IMD3 reduction of 12dB is achieved using the linearization technique. The amount of IMD3 reduction is small

for low levels of output power, because the PA itself becomes more linear.



Figure 13. IMD3 of the PA with and without linearization

#### 5. CONCLUSIONS

A novel linearization technique which utilizes the third-order harmonic to cancel the nonlinearity of the PA output was proposed in this paper. A class-AB CMOS power amplifier with the proposed was designed in  $0.18\mu$ m CMOS process. Experimental results verified the effectiveness of the proposed linearization technique in improving the gain compression and intermodulation distortion.

#### References

[1] P. Andreani, L. Sundstrom, N. Karlsson, M. Svensson, "A Chip for Linearization of RF Power Amplifiers Using Digital Predistortion with a Bit-parallel Complex Multiplier," *Proceedings of the 1999 IEEE Int'l Symp. on Circuits and Systems*, vol. 1, May 1999

[2] J.de.Mingo and A.Valdovinos "Performance of a New Digital Baseband Predistorter using Calibration Memory," *IEEE Trans. on Vehicular Technology*, vol. 50, No. 4, July 2001

[3] K. G. Voyce, J. H. McCandless, "Power Amplifier Linearization Using IF Feedback," *IEEE MTT-S Int'l Microwave Symp. Digest*, June 1989

[4] B. Shi, L. Sundstrom, "Design and Implementation of A CMOS Power Feedback Linearization IC for RF Power Amplifiers," *Proceedings of the 1999 IEEE Int'l Symp. on Circuits and Systems*, pp. I-346-349, June 1999

[5] A. H. Coskun, S. Demir, "A Mathematical Characterization and Analysis of A Feedforward Circuit for CDMA Applications," *IEEE Trans. on Microwave Theory and Techniques*, vol. 51, No. 3, March 2003

[6] C. L. Larose, F. M. Ghannouchi, F.H. Raab, "Optimization of Feedforward Amplifier Power Efficiency on the Basis of Drive Statistics," *IEEE Trans. on Microwave Theory and Techniques*, vol. 51 No. 1, Jan. 2003

[7] D. Jing, W. S. Chan, S. M. Li, C. W. Li, "New Linearization Method using Interstage Second Harmonic Enhancement," *IEEE Microwave* and Wireless Components Letters, vol. 8, No. 11, Nov. 1998

[8] S. Tanaka, F. Behbahani, A. A. Abidi, "A Linearization Technique for CMOS RF Power Amplifiers," *1997 Symp. on VLSI Circuits,* June 1997

[9] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, Cambridge University Press 1998

[10] M. T. Terrovitis, R. G. Meyer, "Intermodulation Distortion in Current-Commutating CMOS Mixers," *IEEE J. Solid-State Circuits*, vol. 35, No. 10, October 2000

[11] C.C. Tang, W.S Lu, L.D. Van, W.S. Feng, "A 2.4-GHz CMOS Down-conversion Doubly Balanced Mixer with Low Supply Voltage," *IEEE Int'l Symp. on Circuits and Systems*, vol. 4, May 2001