Analysis of the PLL Jitter Due to Power/Ground and Substrate Noise

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***Abstract*—Phase-locked loops (PLLs) in radio-frequency (RF) and mixed analog-digital integrated circuits experience substrate coupling due to the simultaneous circuit switching and power/ground (P/G) noise which translate to a timing jitter. In this paper. an analysis of the PLL timing jitter due to substrate noise resulting from P/G noise and large-signal switching is presented. A general comprehensive stochastic model of the substrate and P/G noise sources in very large-scale integration circuits is proposed. This is followed by calculation of the phase noise of the constituent voltage-controlled oscillator (VCO) in terms of the statistical properties of substrate and P/G noise. The PLL timing jitter is then predicted in response to the VCO phase noise. Our mathematical method is utilized to study the jitter-induced P/G noise in a CMOS PLL, which is designed and simulated in a 0.25-μm standard CMOS process. A comparison between the results obtained by our mathematical model and those obtained by HSPICE simulation prove the accuracy of the predicted model.**

***Index Terms*—Cyclostationary noise, jitter, phase-locked loop (PLL), phase noise, power/ground bounce, random process, ring oscillator, substrate noise, voltage-controlled oscillator (VCO).**

I. Introduction

PHASE-locked loops (PLLs) are ubiquitous circuit blocks in RF and mixed-signal integrated circuits. They are extensively utilized as on-chip clock generators to synthesize and de-skew a higher internal frequency from the external lower frequency [1]. In data communications, serial links, and disk-drive read channels, PLL systems are also used as clock recovery systems [1]. In broadband optical communication network,they are used as clock and data recovery (CDR) to generate the clock and retime the data from the received electrical signal [2]–[4]. In wireless communications, they are utilized as frequency synthesizers to synthesize an accurate output frequency [1]. In all of the above applications, the random temporal variation of the phase, or jitter, is one of the most critical performance parameters. Jitter represents the deviation of zero crossings of a periodic waveform from their ideal points on the time axis. The deviation of zero crossings of the waveform synthesized by the PLL causes the setup- and hold-time violations in digital circuits that use the PLL as clock generator, and therefore, leads to data transmission errors and functionality failure.

The ever-increasing demand to integrate all circuit components on the same chip gives rise to some critical noise tolerance requirements for sensitive analog circuits (e.g., PLL circuits) inside the chip. In fact, one of the greatest challenges in the design of a system-on-a-chip (SOC) is the need to place sensitive analog circuits and large complex digital signal processing components on the same die. Due to the high level of interactions between the noisy digital blocks with the noise-sensitive analog portion of the system through various propagation mechanisms, it is highly possible that the large-signal switching transients of the digital circuits corrupt the performance of the analog sub-blocks. In an SOC, coupling from digital circuits into analog components mostly propagates through the common substrate and power/ground (P/G) rails. Substrate and P/G couplings degrade the signal integrity of the PLL in mixed analog-digital integrated circuits where thousands of digital gates may inject noise into the substrate and global P/G wires, especially during clock transitions, introducing hundreds of millivolts of disturbance in the substrate potential [5]–[8]. The peak amplitude and pulse-width of substrate and P/G noise sources are multiple orders of magnitude larger than those of device noise sources in high-speed mixed analog-digital integrated circuits, thereby making substrate and P/G noise sources dominate the performance of PLL circuits. Henceforth, PLL circuits must be designed to operate robustly in the presence of the P/G and substrate noise.

Recently, interesting approaches on characterization of the phase noise in electrical oscillators due to device noise sources have been proposed [9]–[11]. While [9] used a linear time-invariant (LTI) model to describe the behavior of phase noise in oscillators, [10] proposed a more accurate linear time-varying (LTV) model to characterize the oscillator phase noise. [11] studied the phase noise of oscillators by deriving a nonlinear stochastic differential equation for phase error, and solving this equation in the presence of random perturbations. Herzel *et al.* addressed the timing jitter of oscillators due to the power supply and substrate noise [12]. According to [12], an oscillator subject to supply and substrate noise is modeled as a voltage-controlled oscillator (VCO) with different control voltages, and therefore, the jitter effect is viewed as frequency-modulated sinusoidal waveform. The study proposed by [12], however, suffers from an important drawback, where the oscillator circuit in the presence of inherently stochastic substrate and P/G noise sources is treated as a deterministic system. [13] proposed a more general model for the PLL accounting for the time-varying effects of the PLL.

Similar to open-loop oscillators, closed-loop PLL circuits are also susceptible to the external (environmental) noise. Environmental noise sources (e.g., substrate and P/G noise) seriously degrade the performance of a PLL circuit by inducing timing jitter and increasing the limit cycle. As demonstrated by [14],

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the building blocks inside the PLL loop including the VCO, the phase detector, and the frequency divider all contribute to the random phase variations of the output signal. For instance, these noise sources may introduce phase noise in the output signal of the VCO within the PLL, causing unwanted random uncertainties in the synthesized frequency. In the meantime, these noise sources also affect the performance of the phase detector and the frequency divider. With a careful design, the noise contribution of the phase detector, the frequency divider, and the loop filter can be reduced significantly to a tolerable level. The input signal to a PLL is also disturbed by environmental noise sources. In most clock generation applications, however, the VCO of the PLL clock generator is locked to a very low jitter reference input signal generated by an external crystal oscillator. The dominant noise inside the PLL loop is thus contributed by the VCO phase noise.

Recently, Mansuri *et al.* studied the effects of various design parameters of the PLL on the timing jitter and derived some design guidelines to optimize the timing jitter of the PLL [15].

In this paper, we focus on the charge-pump PLL architecture for our analysis due to its widespread application in today's frequency synthesizers for wireless systems and clock generators for microprocessors. The impacts of the P/G bounce and substrate coupling on the PLL timing jitter are investigated. More specifically, the goal of this paper is to predict the timing jitter of the charge-pump PLL circuits in terms of the phase noise of the VCO resulting from the P/G and substrate noise. This is accomplished by using a stochastic model for the P/G noise [16], [17]. The analytical model is verified by simulations of a CMOS PLL circuit designed in a 0.25-μm standard CMOS process surrounded by switching tapered buffers that emulate the large-signal switching of digital circuits. The PLL circuit topology is similar to the one presented in [18].

This paper is organized as follows. In Section II, the block diagram of the PLL system in the presence of all relevant noise sources is briefly illustrated. Section III presents a statistical modeling of substrate noise injected by P/G fluctuations. Section IV studies the VCO phase-noise due to substrate and P/G noise. Section V gives the closed-form analytical model of the PLL timing jitter in response to the VCO phase noise. In Section VI, the simulation results of the PLL timing jitter and comparison with the analytical models are presented. Finally, Section VII provides the concluding remarks.

II. System Modeling for PLL Noise Analysis

The functional block diagram for a charge-pump PLL used in an on-chip clock generation system along with the external clock generator system is shown in Fig. 1. A comprehensive functional description of the charge-pump PLL can be found in many textbooks on analog/RF integrated circuits [19].

The external periodic signal which is normally generated by a crystal circuit, comes as one input of a phase-frequency detector (PFD). The internal clock drives the other input of PFD. The PFD compares the leading edges of its inputs and generates two pulsed signals, *UP* and *DOWN*. The pulsewidths of the *UP* and *DOWN* output terminals depend on the phase deference between the two inputs of the phase detector. The output signals of PFD then drive a charge pump circuit followed by the loop filter. The

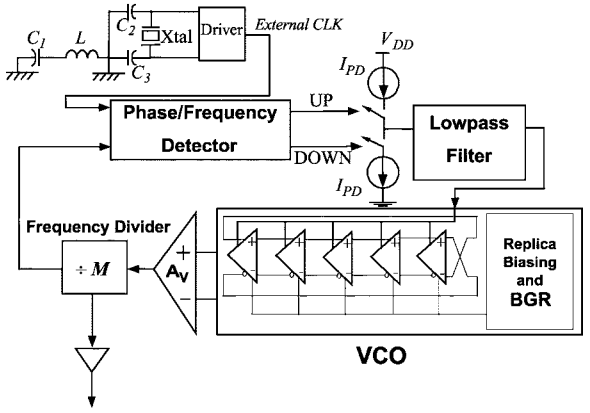

Fig. 1. Functional block diagram of PLL.

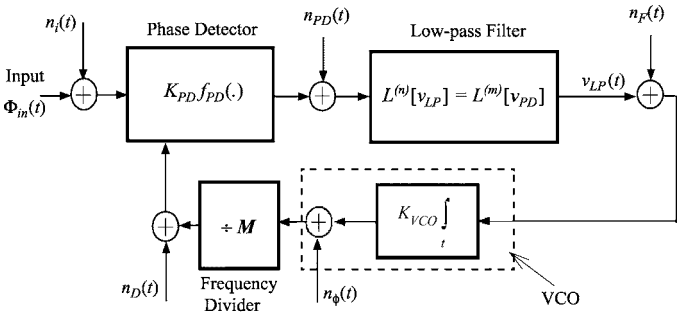

Fig. 2. Functional block diagram of PLL in the presence of all the relevant sources.

charge-pump circuit via two switches either injects, subtracts, or leaves unchanged the charge stored across a capacitor in the loop filter. The output voltage of the loop filter controls the frequency of the VCO. The loop is a negative feedback loop, and if the input frequency is in the *capture range* of the PLL, then after some elapsed time called the *acquisition time*, the PLL is locked to the input frequency.

An important notion regarding the PLL circuit of Fig. 1 is that the VCO exhibits a finite power-supply rejection (PSR). Substrate noise resulting from the P/G bounce and simultaneous switching of digital circuits in an SOC thus induces a nonzero timing jitter at the output signal of the VCO. More precisely, substrate and P/G noise cause jitter accumulation due to inherent integration taking place in the VCO. Jitter accumulation in turn leads to synchronization failure in the whole system. The goal of this paper is to analyze the PLL timing jitter due to substrate and P/G noise, and propose a closed-form analytical model to predict this jitter.

The system block diagram of a PLL along with various random noise sources resulting from P/G and substrate noise couplings is shown in Fig. 2. The average power-spectral densities (PSD) of environmental noise sources, such as P/G and substrate noise are much greater than those of device noise sources, such as thermal noise. As a result, the PLL jitter due to various device noise sources is negligible compared to the jitter due to the environmental noise sources.

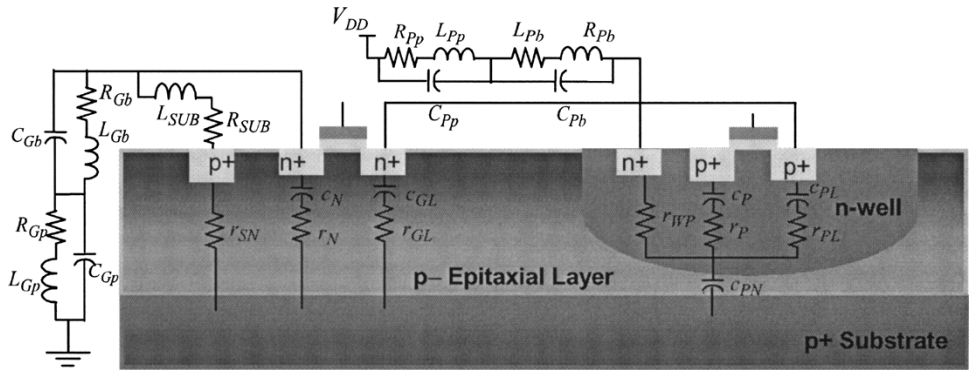

Fig. 3. Cross-sectional view of a static CMOS inverter along with chip-package interface parasitics.

In general, all constituent loop components may contribute noise and jitter to the PLL output. The effect of noise on the phase detector performance has been studied in [20]. The phase detector is not, however, a major noise contributor to the PLL phase noise and jitter. The phase detector fluctuations due to P/G and substrate noise are largely attenuated using a differential architecture, and also by means of the PLL loop filter [20]. As a result, timing jitter in a PLL is mainly associated with two important noise sources induced by P/G and substrate noise:

- noise at the input $n_i(t)$;
- phase noise of the VCO, $n_\phi(t)$.

The loop bandwidth as well as the peaking of the loop frequency response of the PLL determines which noise source has the dominant impact on the PLL timing jitter. The noise at the input propagates through the same signal path as the input signal to the PLL. Therefore, the noise transfer function for the input noise is identical to the signal transfer function. This means that a narrowband lowpass filter eliminates the higher frequency components of the input noise and reduces the impact of the input noise source on the timing jitter. On the other hand, the PLL operates as a highpass filter for the VCO noise [19], meaning that, in contrast to the input noise, a narrow-band loop filter is not a good choice for the VCO phase noise attenuation.

Previously, more attention was paid to understanding the effect of the input noise source on the PLL performance [1], which is also easier to characterize than the impact of the VCO phase noise induced by substrate and P/G noise on the PLL jitter. Furthermore, for both clock synthesizers and high performance clock recovery systems, an accurate analysis of the output jitter due to the internal VCO phase noise is important.

Considering the general case of having an nth-order loop filter, the characteristic nonlinear differential equation of a PLL is as follows:

$$L^{(n)}\left[\frac{2\pi(f_{\rm VCO}-f_0)}{K_{\rm VCO}}\right] = L^{(m)}\left[K_{\rm PD}f_{\rm PD}\left(\Phi_{in}(t)-\frac{2\pi}{M}\int_t\left(f_{\rm VCO}+\frac{1}{2\pi}\frac{dn_\phi}{dt'}\right)dt'\right)\right] \quad (1)$$

where f_0 and $f_{\rm VCO}$ are the VCO center and output frequencies, respectively. Φ_{in} is the input reference phase, $f_{\rm PD}(\Phi)$ represents the phase detector function, and $n_\phi(t)$ represents the phase noise of the VCO.

III. Substrate and P/G Noise Characterization

Substrate noise and P/G bounce are predominant environmental noise sources in mixed analog-digital integrated circuits [6], [21]. Since a dominating component of the substrate noise injection is due to the leakage of the voltage bounce on the supply/return path, an accurate circuit model for substrate noise must incorporate the circuit model for the noisy supply and ground rails, a phenomenon that was not considered in previous researches. Reference [21] considered the contribution of supply noise injection on the substrate noise ignoring the noise caused by the large-signal switching transients in the digital circuit. On the other hand, [22] focused on the substrate coupling induced by the large-signal switching transients of the circuit, neglecting the P/G bounce. *An accurate analytical study of substrate noise should include both the direct coupling as well as the coupling due to fluctuations on the power and ground rails.*

In this section, an efficient model for substrate noise due to direct coupling of switching circuits as well as fluctuations on the P/G rails coupling is developed. The proposed analytical model will contain the statistical nature of the switching activity of digital circuits. The model is germane to epi-type heavily doped substrate used in mixed-signal circuits. Note that this model is less accurate compared to 3D models proposed in [23]. However, the advantage of the proposed model is that it can appropriately be incorporated in the PLL analytical models developed in this paper.

In a CMOS mixed analog-digital integrated circuit, the substrate is normally composed of a lightly doped epitaxial layer grown on a heavily doped substrate in order to minimize the transistor latch-up [5]. In an epi-type substrate technology, the injected lateral current from the source of a digital circuit (e.g., a CMOS inverter) flows through the heavily doped substrate material because of its low resistivity compared to the inter-layer silicon or epitaxial layer [5]. The bulk can thus be modeled as a *single electrical node* for any given technology (see [5]). Shown in Fig. 3 is the cross sectional view of a static CMOS inverter along with all electrical parasitics resulting from interactions between semiconductor materials with different doping concentrations. Fig. 3 also includes the electrical parasitics of the P/G wires and the chip-package interface. According to this figure, the chip's pin parasitics are represented by an *RLC* circuit (R_{Pp}, L_{Pp}, C_{Pp}) for the power supply pin, and an RLC

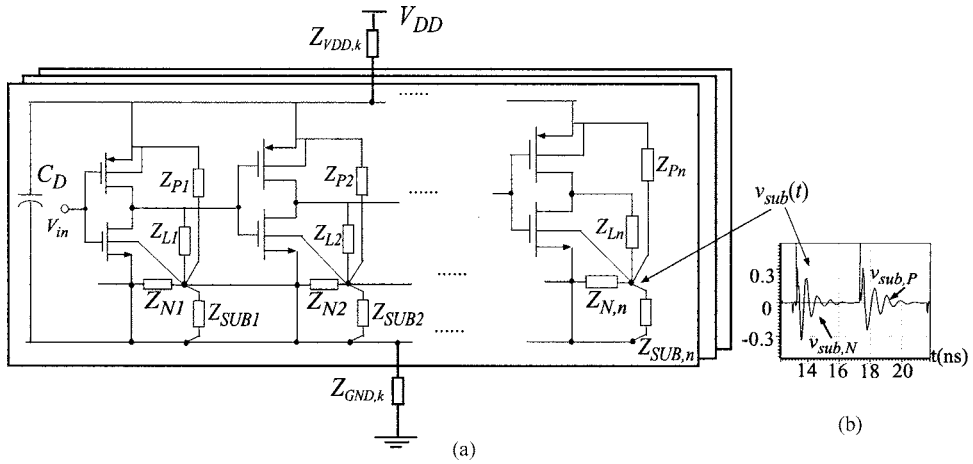

Fig. 4. (a) Circuit consisting of multistage tapered buffers for substrate noise injection. (b) Substrate noise waveform.

circuit (R_{Gp}, L_{Gp}, C_{Gp}) for the ground pin. The parasitics introduced by bondwires and die pads are also modeled as an *RLC* circuit (R_{Pb}, L_{Pb}, C_{Pb}) for the power supply connection, and an *RLC* circuit (R_{Gb}, L_{Gb}, C_{Gb}) for the ground connection. Currents flowing through the bondwires and pin-to-die interface exhibit large slew-rates during output transitions, hence the supply voltage waveform seen by the on-chip circuitry experiences a large amount of switching noise.

Fig. 4(a) depicts the circuit schematic being utilized to generate the substrate noise injection in an epitaxial CMOS technology.

The circuit is comprised of 40 1-pF capacitors each driven by 6-stage CMOS tapered buffers in 0.25-μm CMOS technology. To reduce the simultaneous switching noise, every ten tapered buffers are connected to a single ground and supply pin. Electrical parasitics seen in regard to a single inverter are included in the circuit to accurately model the substrate and P/G wires. More precisely, in Fig. 4(a), $Z_{\mathrm{VDD},k}$, $Z_{\mathrm{GND},k}(k = 1, \cdots, 4)$ are P/G impedances modeling the chip-package interface parasitics including the chip bondwires and package traces. These impedances are highly inductive, as also depicted in Fig. 3 for a single inverter. $Z_{\mathrm{SUB},i}(i \in [1, n])$ represents the equivalent substrate impedance consisting of the substrate bias resistance and inductance, respectively. $Z_{N,i}$ is the equivalent impedance from the chip ground to the heavily doped substrate including the wiring capacitance and junction capacitance of NMOS device. $Z_{P,i}$ is the equivalent impedance from the chip power supply to the heavily doped substrate including the nwell junction capacitance and the nwell physical resistance. $Z_{L,i}$ is the equivalent load impedance including the gate capacitance of the following fan-out stages. C_D is the on-chip bypass[1] (decoupling) capacitor used to reduce the P/G bounce. Since the substrate is tightly coupled to the return path by distributed surface substrate contacts, the voltage bounce arising from logic switching, especially on the ground path, appears as substrate noise. Fig. 4(b) shows the substrate noise for a complete one-cycle simultaneous switching of the buffers. The underdamped oscillatory behavior of substrate coupling injected by the P/G bounce is due to the highly inductive behavior of the bondwires and on-chip interconnects at high frequencies.

Substrate noise resulting from fluctuations on the on-chip power supply lines and ground wires due to signal switching of output buffers can have excessively large values when multiple output drivers switch simultaneously, as also considered in Fig. 4(a). Power and ground fluctuations are out of phase, therefore, the P/G noise is, in fact, the algebraic summation of ringings on the power and ground rails. The P/G bounce is the main source of substrate noise, which causes logic and timing failure in the circuits. To reduce the P/G bounce, which is a high frequency waveform, on-chip bypass capacitors have to be placed in close proximity of output buffers, as also shown in Fig. 4(a). In practice, bypass capacitors can be placed at any location that is free after floorplanning. On-chip bypass capacitors across output buffers make the supply fluctuations in phase with the ground fluctuations, and remove high frequency components from supply and ground variations. In the time domain, an on-chip bypass capacitor smooths out the variations on power supply and ground wires that would have otherwise been spike-like waveforms. In the frequency domain, it shrinks the spectral bandwidth of the variations. Reference [6] provides a comprehensive study of the effect of on-chip bypass capacitors and the mathematical relationship between the peak value of the P/G noise and required capacitance value to reduce the P/G noise.

In order to characterize the statistics of substrate coupling due to the circuit switching and P/G noise, an observation is made that is based on actual experimental measurements carried out in [5]. In a lightly doped epitaxial layer grown on a heavily doped substrate, if the analog and digital circuits are separated by at least four times the thickness of the epitaxial layer, the resistance between the substrate contacts will be independent of their separations [5]. Therefore, the spacing between the switching blocks causes solely a random phase shift on the noise fluctuations. On the other hand, the peak amplitudes of damped oscillations for each noise waveform $v_{\mathrm{sub},N}(t)$ and $v_{\mathrm{sub},P}(t)$, [cf. Fig. 4(b)] are a function of switching activities of digital circuits and are thus represented by *discrete-time* random processes.

[1]Another terminology for bypass capacitor is decoupling capacitor, which is more commonly used by circuit designers. Fundamentally, a bypass component is a shunt component. Decoupling is the isolation of two circuits on a common line. It is accomplished by inserting a filter in series with the line. Therefore, a decoupling element must be a series element.

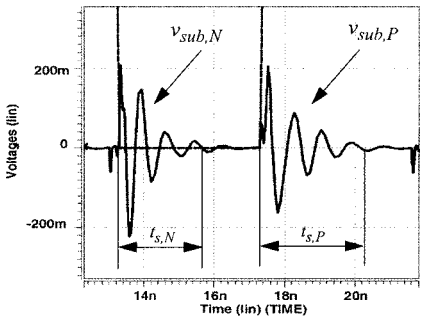

Fig. 5. Substrate noise coupling.

The above observations help us derive a mathematically robust and efficient stochastic model for substrate noise, as follows:

$$v_{\text{sub}}(t) = \sum_{n=-\infty}^{\left[\frac{t}{T}\right]} A_{\text{sub},N}[n] v_{\text{sub},N}(t - nT - \lambda_n) + \sum_{n=-\infty}^{\left[\frac{t}{T}\right]} A_{\text{sub},P}[n] v_{\text{sub},P}\left(t - nT - \frac{T}{2} - \gamma_n\right). \quad (2)$$

Substrate noise is comprised of two additive terms. The first term is due to the low-to-high signal transition, and the second one is due to the high-to-low signal transition, as depicted in Fig. 5.

$A_{\text{sub},N(P)}$ is a discrete-time random process that accounts for the number of adjacent switching circuits switching simultaneously. λ_n and γ_n are a set of uniformly distributed independent random variables in the interval $[0, T]$ (T is the clock cycle-time). Their presence in the noise expression is because the digital circuits switch randomly across the chip. The random switching of the digital circuits located at different locations across the chip are directly translated to random signal propagation delays toward the sensitive analog terminals inside the chip. The analysis can easily be extended to a more general scenario in which there are multiple synthesized frequencies across the chip.

To obtain the PSD of substrate noise $v_{\text{sub}}(t)$, the following Theorem is used.

Theorem 1 ([24, p. 374]): Consider the following wide-sense cyclo-stationary stochastic process:

$$x(t) = \sum_{n=-\infty}^{\infty} A[n] v(t - nT)$$

where $A[n]$ is a discrete-time random-process. The shifted process $z(t)$, given below

$$z(t) = \sum_{n=-\infty}^{\infty} A[n] v(t - nT - \lambda_n)$$

is a wide-sense stationary process, whose PSD is

$$\overline{S_z(\omega)} = \frac{1}{T} S_A(e^{j\omega}) |V(\omega)|^2. \quad (3)$$

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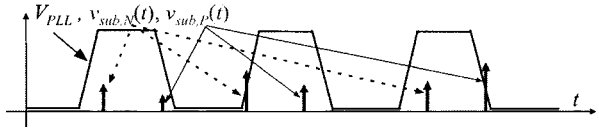

Fig. 6. Substrate noise modeled as stochastic impulse train.

Using Theorem 1 and (3) the PSD of substrate noise $v_{\text{sub}}(t)$ is obtained as follows:

$$S_{\text{sub}}(\omega) = \frac{1}{T}\left[S_{A_{\text{sub},N}}(e^{j\omega}) |V_{\text{sub},N}(\omega)|^2 + S_{A_{\text{sub},P}}(e^{j\omega}) |V_{\text{sub},P}(\omega)|^2\right]. \quad (4)$$

Applying (4) on a special example for substrate noise proves useful in forthcoming discussions. This example includes the case in which the ringing duration of substrate noise is small compared to the duty cycle of the synthesized signal of the PLL. In this case, the substrate noise is accurately modeled as impulse train with normally distributed random area and a uniformly distributed random time-shift to account for the switching activity and random signal propagation delay, respectively. Consequently, the noise expression in (2) is simplified to a stochastic impulse train specified by (5), and depicted in Fig. 6

$$v_{\text{sub,impulse}}(t) = \sum_{n=-\infty}^{\left[\frac{t}{T}\right]} A_{\text{sub},N}[n]\delta(t - nT - \lambda_n) + \sum_{n=-\infty}^{\left[\frac{t}{T}\right]} A_{\text{sub},P}[n]\delta\left(t - nT - \frac{T}{2} - \gamma_n\right). \quad (5)$$

The PSD of substrate noise for this particular example simplifies to

$$S_{\text{sub,impulse}}(\omega) = \frac{1}{T}\left[S_{A_{\text{sub},N}}(e^{j\omega}) + S_{A_{\text{sub},P}}(e^{j\omega})\right]. \quad (6)$$

The above analytical model is used in Sections IV and V to derive the VCO phase noise and the PLL timing jitter.

IV. VCO Phase-Noise Analysis

As described in Section II, the VCO (and in particular, the ring VCO) is the most noise-sensitive circuit among other sub-blocks in a PLL circuit. The reason is that the ring VCO is a closed-loop oscillator where corrupted zero-crossings of the oscillations due to substrate and supply noise are recirculated in the loop. Moreover, fast jitter components generated by the VCO are not suppressed by the PLL (the PLL operates as a high-pass filter to the VCO noise input). On the other hand, the jitter coming from the input terminal does not have much of an effect because firstly, in a PLL-based clock generator the input is coming from a very low-jitter source, and secondly, the PLL loop filter eliminates the in-band components of the input jitter.

The VCO phase noise analysis is carried out by studying a simple conventional differential delay stage commonly used in a ring VCO. To understand the substrate noise effect on the VCO operation, consider a four stage fully differential ring oscillator-based VCO shown in Fig. 7 [18].

The VCO incorporates a replica biasing circuitry that always biases the delay element such that the output voltage swing of each differential delay stage is fixed and independent of supply

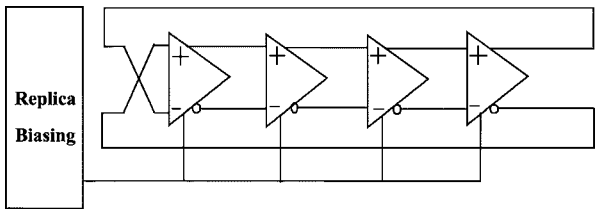

Fig. 7. VCO based on differential ring oscillator with the voltage controlled resistor and replica biasing.

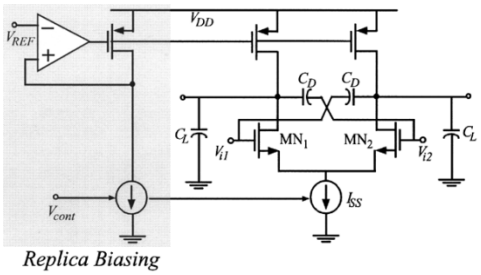

Fig. 8. A simple differential delay stage.

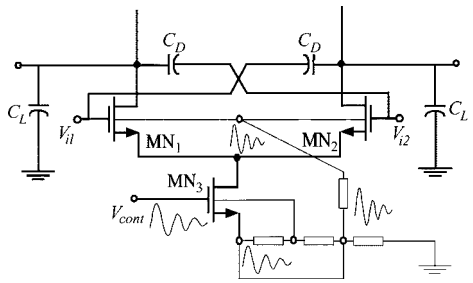

Fig. 9. Substrate injection mechanism for a differential delay stage.

variation. Shown in Fig. 8 is the circuit topology of a differential delay stage being incorporated in the implementation of Fig. 7. The capacitor pair C_D has been employed to neutralize the feed-forward transition provided by C_{GD} of the MOS devices. Each MOS transistor of the differential source-coupled pair experiences a large-signal gate voltage and therefore, it experiences multiple transitions in its region of operation. Moreover, the $I_D - V_{\rm GS}$ relationship of a MOS transistor is nonlinear for both triode and saturation regions. All these phenomena cause the VCO frequency to be a nonlinear function of the supply and input control voltages. This nonlinear relationship is also dependent on the circuit topology being adopted for a delay stage, however, as will be seen later in this section, the general relationship between the excess VCO frequency and substrate noise remains approximately the same. In most of today's differential ring oscillator architectures the VCO gain is controlled by the tail current which makes it possible to have a wider tuning range and a pseudo-linear frequency-voltage relationship.

The noise propagated through the substrate due to the P/G bounce and large-signal switching appears as a common-mode signal for the differential pair transistors, thus does not affect the delay and dynamic operation of the differential pair (cf. Fig. 9). On the other hand, substrate noise affects $I_{\rm SS}$ through both the control path and the direct coupling to the tail current's transistor, as shown in Fig. 9. The former component is attenuated by using a differential control input while the latter being almost intact. Using the BSIM3v3 MOS model, the tail current $I_{\rm SS}$ is:

$$I_{\rm SS} = W v_{\rm sat} C_{\rm ox} (V_{\rm GS} + V_{\rm TH} - V_{\rm DS,sat}) \tag{7}$$

$$V_{\rm DS,sat} = (1-\kappa)(V_{\rm GS} - V_{\rm TH}) \tag{8}$$

$$\kappa = \frac{1}{1+\frac{E_{\rm sat}}{E}} = \frac{1}{1+\frac{E_{\rm sat}L}{(V_{\rm GS}-V_{\rm TH})}} \tag{9}$$

Direct coupling

Coupling through control path

$$I_{\rm SS} = W v_{\rm sat} C_{\rm ox} (V_{\rm cont} + v_{\rm cont,sub} - v_{tr,sub} - V_{\rm TH} - V_{\rm DS,sat}). \tag{10}$$

In (7), $V_{\rm DS,sat}$ is the drain–source voltage at which the velocity saturation occurs, and $\nu_{\rm sat}$ is the saturated drift velocity. In (8), κ measures the degree of velocity saturation (with E the longitudinal electric field). $E_{\rm sat}$ is the electric field when the velocity saturation comes into play.

Since the velocity-saturated drain–source voltage, $V_{\rm DS,sat}$, is also a nonlinear function of the gate-source voltage, the tail current becomes a nonlinear function of substrate noise which introduces harmonic distortion at the VCO output.

To quantify the VCO phase noise, and, subsequently, the PLL jitter induced by substrate noise, we first obtain the VCO phase noise in response to substrate noise variations. For the ultimate design criteria of having a small coupling from the substrate material and P/G rails to the PLL circuit we can simplify (10) and derive the autocorrelation function of excess frequency variation in terms of the autocorrelation of substrate noise. Starting with (10), the current variations of the tail current due to substrate noise is equal to

$$\Delta I_{\rm SS,noise} = W v_{\rm sat} C_{\rm ox} \kappa_\Delta v_{\rm sub}$$

$$\text{assuming} \qquad v_{\rm sub} < (V_{\rm cont} - V_{\rm TH})$$

$$\text{where} \qquad \kappa_\Delta \approx \frac{L E_{\rm sat}}{(V_{\rm cont} - V_{\rm TH})} \kappa^2 \tag{11}$$

where $v_{\rm sub}$ accounts for the total contributions of coupled noise on the control input line and coupled noise through the substrate bulk. The assumption in (11) is readily satisfied by placing on-chip bypass capacitors across the large current drivers.

Note that each delay stage inside the ring VCO is driven by a similar delay stage, and is driving another similar delay stage. The large-signal input applied to the differential pair causes the bias points of differential pair transistors to vary periodically. The output differential current is a nonlinear function of the instantaneous input voltage and the tail current. Differential operation reduces the noise to a great extent. Nonetheless, the large-signal operation of a ring VCO influences the overall VCO sensitivity to substrate noise. This leads to another phenomenon, that is, the tail current's fluctuation induced by substrate noise results in a differential additive voltage noise at the differential output node of each differential delay stage. The following analysis proves this observation.

The output current of the differential delay stage in Fig. 8 is a function of the instantaneous differential input voltage $V_{id} = V_{i1} - V_{i2}$ to the delay stage and the current at the output of the tail current $\Delta I_{\rm SS,noise} + I_{\rm SS}$, with $I_{\rm SS}$ being the noise-free current:

$$I_o = I_{D1} - I_{D2} = F(V_{id}, I_{\rm SS} + \Delta I_{\rm SS,noise}). \tag{12}$$

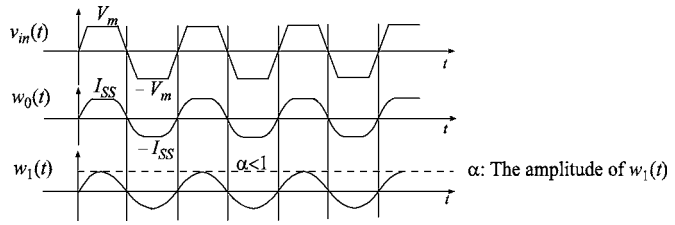

Fig. 10. $w_0(t)$ and $w_1(t)$ waveforms.

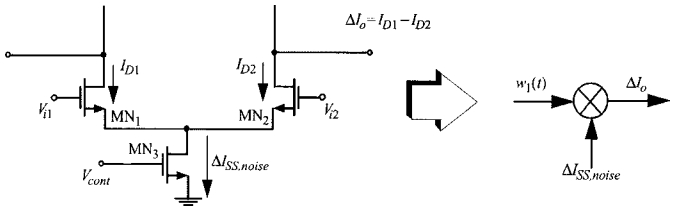

Fig. 11. Differential delay stage modeled as a mixer.

Assuming $\Delta I_{\mathrm{SS,noise}} \ll I_{\mathrm{SS}}$, the first-order Taylor series expansion leads to the following expression [25]:

$$I_o = F(V_{id}, I_{\mathrm{SS}}) + \frac{\partial F(V_{id}, I_{\mathrm{SS}})}{\partial (I_{\mathrm{SS}} + \Delta I_{\mathrm{SS,noise}})} \Delta I_{\mathrm{SS,noise}} \quad (13)$$

or

$$I_o = w_0(t) + w_1(t) \Delta I_{\mathrm{SS,noise}} \quad (14)$$

where $w_0(t)$ and $w_1(t)$ are two periodic waveforms running at the VCO frequency f_{VCO}, as also depicted in Fig. 10.

From the tail current's fluctuations perspective, the differential pair is thus modeled as a mixer as depicted in Fig. 11.

The nonlinear operation of the differential pair is modeled using an instantaneous current gain $w_1(t)$, which is a periodic function of time, as shown in Fig. 11. The instantaneous current gain, $w_1(t)$, is expressed in terms of the instantaneous transconductances of switching devices, MN1 and MN2

$$w_1(t) = \frac{g_{m1}(t) - g_{m2}(t)}{g_{m1}(t) + g_{m2}(t)} \quad (15)$$

where $g_{m1}(t)$ and $g_{m2}(t)$ represent the instantaneous small-signal transconductances of MN1 and MN2. To account for the short-channel effects, the instantaneous transconductance g_m of a transistor in terms of its dc bias current I_{DQ} is derived using BSIM equations

$$g_m = \frac{2I_{DQ}}{V_{\mathrm{GS}} - V_{\mathrm{TH}}} \left[\frac{\frac{(V_{\mathrm{GS}} - V_{\mathrm{TH}})}{2} + LE_{\mathrm{sat}}}{V_{\mathrm{GS}} - V_{\mathrm{TH}} + LE_{\mathrm{sat}}} \right]. \quad (16)$$

The output differential current resulting from the tail current's fluctuations flows through the load generating differential voltage at the output. The overall differential voltage of the kth stage thus becomes

$$V_{out}(t) = V_{\mathrm{REF}} \cdot s_{\mathrm{VCO}}^{(k)}(t) - \left(\frac{V_{\mathrm{DD}} - V_{\mathrm{REF}}}{I_{\mathrm{SS}} + \Delta I_{\mathrm{SS,noise}}} \right) \Delta I_{\mathrm{SS,noise}} w_1^{(k)}(t) \quad (17)$$

where $s_{\mathrm{VCO}}^{(k)}$ is the noise-free VCO signal with unit amplitude associated with the kth stage. Also, $w_1^{(k)}$ is the instantaneous current gain of the kth stage. The output voltage of each differential pair will be the large-signal input to the following delay stage controlling the switching action of the switching pair. The modulating noise on the input signal to each delay stage has a negligible contribution to the differential output of the stage compared to the coupled noise from the tail current. The reason is that the differential transconductance is nonzero only in a small transition region around the zero-crossing points of the input differential voltage, where the switching devices are in the saturation region [26]. In this small transitional interval, the input signal variation attains its maximum rate of change, therefore, the modulating substrate noise from the previous stage will have a negligible effect. A significant differential component of noise and fluctuations for each delay stage of the ring VCO is due to the variations of the tail current of that stage induced by the substrate noise. These observations are verified using an HSPICE simulation of a 4-stage differential ring VCO circuit, where each stage delay stage is shown in Fig. 8. Fig. 12(a) and (b) compares the differential output waveforms of the first and the third delay stages in Fig. 7 with and without substrate noise. As observed in Fig. 12(a) and (b), modulating fluctuation on the differential output signal of each stage are mainly dominated by the noise of that stage. Shown in Fig. 12(c) is a comparison between the spectrum of the differential output of the third stage with and without substrate noise. Two important phenomena are observed. First, the phase noise of the VCO output is significantly increased. Secondly, a noise-induced frequency shift in the center frequency is taking place, affecting the accuracy of the PLL that incorporates this VCO.

Proved by both the analytical study equation (17) and simulations, the tail current's fluctuations induced by substrate noise thus appears as an additive noise at the differential output voltage of each delay stage.

To predict the VCO phase noise induced by substrate noise, the VCO frequency is first calculated. Fig. 13 shows the kth stage in a chain of N stage differential ring-VCO along with the capacitors that contribute to the delay calculation.

The common node s_{k+1} shown in Fig. 13 experiences a double-frequency variation compared to the voltage variations at the gate terminals of switch-pair transistors [19]. The input capacitance seen at the gate terminal of the $(k+1)^{\mathrm{st}}$ stage is therefore expected to be slightly smaller than the gate-source capacitance $C_{\mathrm{GS},k+1}$. Ignoring the channel length modulation in MOS devices, and assuming the gate terminals of the $(k+1)^{\mathrm{st}}$ stage to have fully differential voltages, the current-voltage relationship at each gate terminal of the $(k+1)^{\mathrm{st}}$ stage is expressed as follows:

$$I_{G,k+1,i} = \left[C_{\mathrm{GS},k+1} + \frac{C_{\mathrm{SS},k+1}}{2} \frac{V_{in,k+1,i}}{\sqrt{2V_{\mathrm{in,max}}^2 - V_{in,k+1,i}^2}} \right] \times \frac{dV_{in,k+1,i}}{dt} \quad i = 1, 2 \quad (18)$$

where $V_{\mathrm{in,max}} = \sqrt{0.5 I_{\mathrm{SS}} / (\mu_n C_{\mathrm{ox}} (W/L))}$. Equation (18) states that the large-signal input impedance of the differential pair can be defined using a nonlinear voltage-dependent

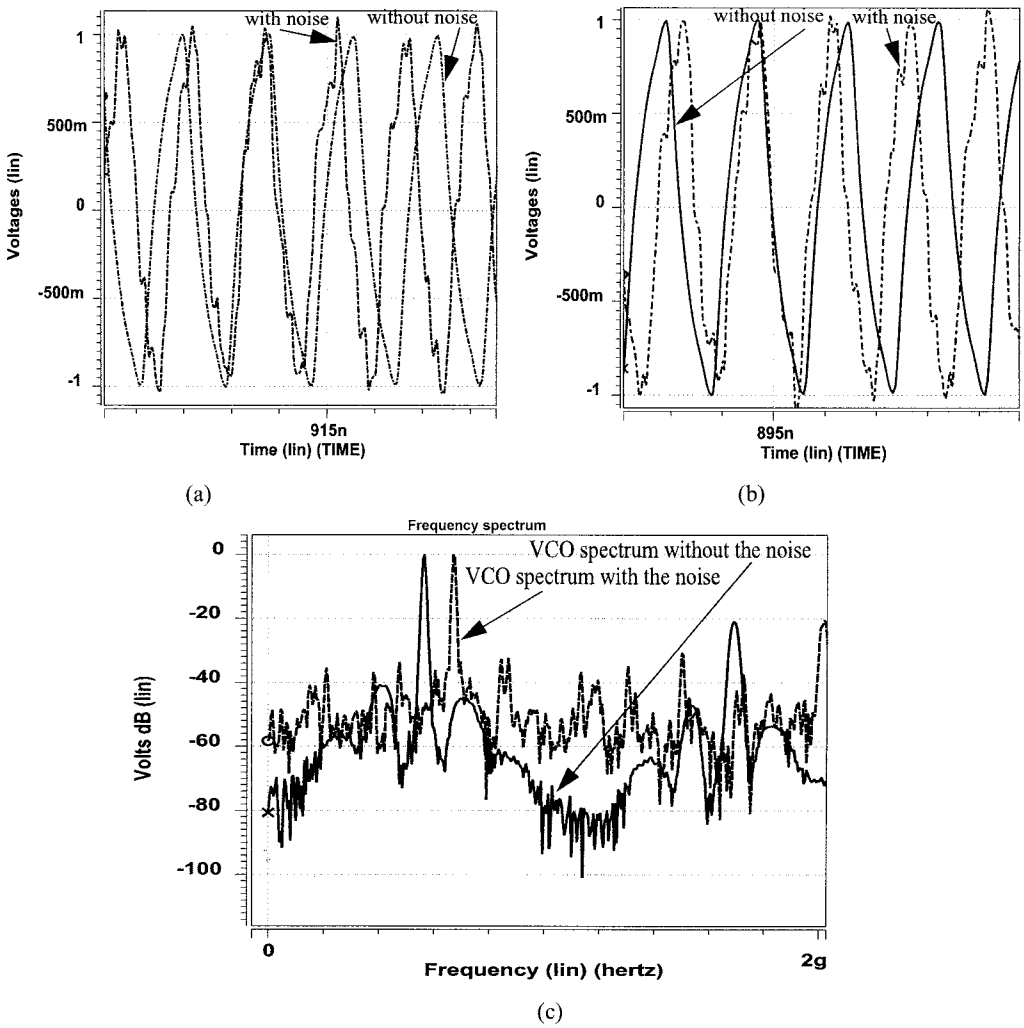

Fig. 12. (a) Differential output voltage of the first stage. (b) Differential output of the second stage. (c) Output spectrum of the third stage with and without substrate noise.

capacitance. The value of this input capacitance is a function of the input voltage, thereby varying with time. Assuming a sinusoidal input with the amplitude of $V_{\text{in,max}}$, the time average of this capacitance is calculated as follows:

$$\begin{aligned} C_{\text{eff},k+1} =& C_{\text{GS},k+1} + \frac{4}{T} \\ & \times \left(\int_0^{\frac{T}{4}} \frac{C_{\text{SS},k+1}}{2} \frac{V_{in,k+1,i}}{\sqrt{2V_{\text{in,max}}^2 - V_{in,k+1,i}^2}} dt \right) \\ \cong& C_{\text{GS},k+1} - \frac{C_{\text{SS},k+1}}{2\pi} \ln(3+2\sqrt{2}) \end{aligned} \tag{19}$$

where $\ln(x)$ represents the natural logarithm of x. Using (19), the 50% delay of the kth stage *under a step input* is calculated as follows:

$$t_{d,k} = 0.69 R_{o,k}(C_{\text{DB},k} + C_{\text{eff},k+1} + C_{\text{ext}}) \tag{20}$$

where $R_{o,k}$ is the output resistance of the kth stage, and C_{ext} is an external capacitance added to achieve the desired VCO center frequency. Since PMOS transistors are biased to be in the triode region, $R_{o,k}$ is approximately equal to the PMOS output resistance. Assuming identically matched delay stages, the VCO output frequency is given as follows:

$$\begin{aligned} & f_{\text{VCO}} \\ &= \frac{1}{n_c N R_{oP} C_L} \\ &= \frac{1}{n_c N R_{oP}(C_{\text{DB}} + C_{\text{GS}} - 0.28C_{\text{SS}} + C_{\text{ext}})} \\ &= \frac{I_{\text{SS}}}{n_c N (V_{\text{DD}} - V_{\text{REF}})(C_{\text{DB}} + C_{\text{GS}} - 0.28C_{\text{SS}} + C_{\text{ext}})} \end{aligned} \tag{21}$$

where n_c is the constant coefficient, which in the case of the delay stage of Fig. 8 is 1.38.

Both C_{DB} and C_{SS} are nonlinear functions of substrate noise, thereby making f_{VCO} to be a nonlinear function of substrate noise. Nonetheless. this nonlinear dependence has a negligible contribution to the phase noise. This is proved by deriving an upper bound for the load capacitance C_L in the presence of substrate noise. To arrive at such upperbound, we calculate the first-order truncation of Taylor series expansion of the overall nonlinear junction capacitance, $C_{\text{DB}} - 0.28C_{\text{SS}}$, with respect

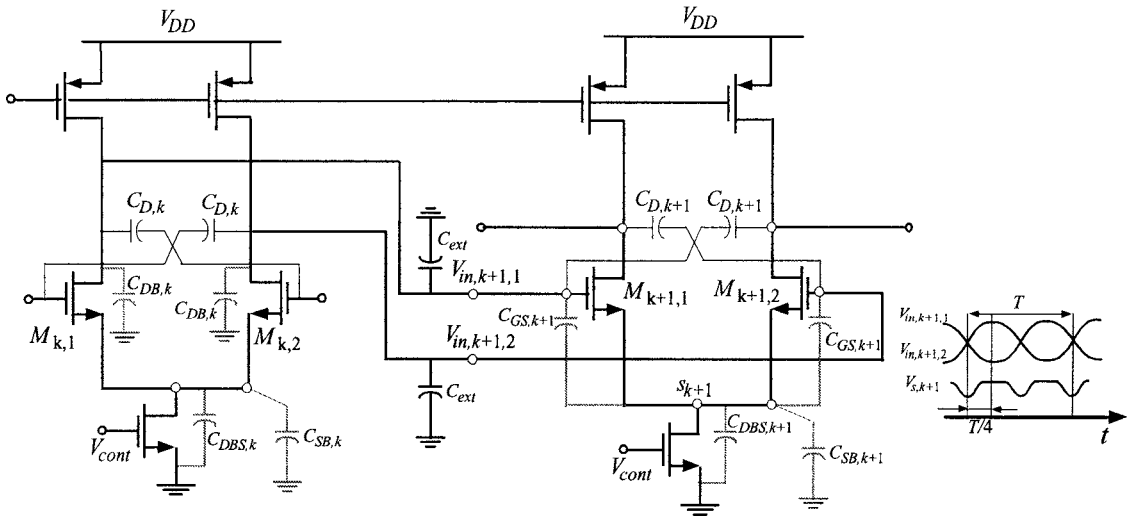

Fig. 13. The kth and $(k+1)^{\text{st}}$ stages of a differential ring VCO along with the parasitic capacitances.

to the substrate noise. Using this approach, an upperbound for the load capacitance is

$$C_L < C_{L0}\left[1+\left|\left(\frac{C_{L0}-C_{\rm GS}-C_{\rm ext}}{C_{L0}}\right)\frac{mv_{\rm sub}}{\phi_B}\right|\right] \tag{22}$$

where C_{L0} is the total load capacitance with a zero-valued substrate noise, m is the junction coefficient ($0.3 < m < 0.45$), and ϕ_B is the build-in potential. The second additive term is very small compared to unity for given sub-micron technology, which justifies our assumption of ignoring the effect of substrate noise on junction capacitances.

Having obtained the current variation of the tail current due to substrate noise, the excess VCO frequency in terms of the substrate voltage is readily calculated, i.e.,

$$\begin{aligned}\Delta f_{\rm VCO} &= \left[\frac{Wv_{\rm sat}C_{\rm ox}\kappa_\Delta}{n_cNC_L(V_{\rm DD}-V_{\rm REF})}\right]v_{\rm sub}(t)\\ &= K_{\rm VCO,noise}v_{\rm sub}(t)\end{aligned} \tag{23}$$

where $v_{\rm sub}(t)$ is characterized by (2). Substrate noise therefore modulates the current gain $w_1(t)$ of the differential delay stage, thereby making the VCO excess frequency to be a cyclo-stationary process. Hence, the VCO excess frequency becomes $\Delta f_{\rm VCO} = K_{\rm VCO,noise}v_{\rm sub}(t)$. The general form of (17) holds true for any arbitrary differential stage, while $K_{\rm VCO,noise}$ varies with the circuit topology.

The time-average of autocorrelation function of the VCO excess frequency, $R_{f_{\rm VCO}}(\tau)$, is a stationary process [24], and can be derived as

$$\begin{aligned}R_{f_{\rm VCO}}(\tau) &= \langle E\left\{\Delta f_{\rm VCO}(t)\Delta f_{\rm VCO}(t+\tau)\right\}\rangle_t\\ &= K^2_{\rm VCO,noise}R_{\rm sub}(\tau)\end{aligned} \tag{24}$$

where $\langle\cdot\rangle_t$ represents the time-average operator. $R_{\rm sub}(\tau)$ represents the autocorrelation of substrate noise $v_{\rm sub}(t)$ whose Fourier transform is the noise PSD, $S_{\rm sub}(\omega)$. The time-average autocorrelation of the VCO excess frequency variation is a linear function of the autocorrelation of the P/G noise. The time-average PSD of the VCO excess phase is referred to as the *phase noise*. Consequently, the phase noise of the VCO induced by substrate noise is obtained using the following equation:

$$\begin{aligned}&S_{\Phi_{\rm VCO}}(\omega)\\ &= \mathsf{F}\left\{R_{\Phi_{\rm VCO}}(\tau)\right\}\\ &= \mathsf{F}\left\{E\left\{\frac{1}{T^2}\int_{t-T}^{T}\int_{t+\tau-T}^{T}\Delta f_{\rm VCO}(t_1)\Delta f_{\rm VCO}(t_2)dt_1dt_2\right\}\right\}\\ &= \frac{K^2_{\rm VCO,noise}}{\omega^2}S_{\rm sub}(\omega)\end{aligned} \tag{25}$$

where $\mathsf{F}\langle\cdot\rangle$denotes Fourier transformation. $S_{\rm sub}(\omega)$ is the PSD of substrate noise given by (4) [or (6) in the simplified case of having impulsive noise]. The simplified linear relationship between substrate noise and the incremental current variation of the tail current allows one to consider the effect of substrate noise as an additive noise in the closed-loop PLL system, however with a different VCO gain, $K_{\rm VCO,noise}$. This will be investigated in Section V.

As mentioned in Section I, the focus of this paper is on the phase-noise analysis due to substrate and P/G noise. Among other practical issues contributing to the VCO and PLL phase noise, the device mismatch is perhaps the most important component. The analysis undertaken in this section assume that all devices are identically matched. In practice, small inaccuracies in manufacturing process introduce device mismatches. Mismatches cause three major effects on the performance of the circuits, and in particular the delay stages within a ring-VCO [19]: 1) dc offset; 2) finite even-order distortion; 3) lower common-mode rejection. Details about each of these effects can be found in [19]. In [27], we have established an analogy between the offset and device noise. In the noise analysis of integrated circuits, the effect of all noise sources in the circuit are referred back to the input, and is represented by input referred noise sources [19]. The input-referred noise sources indicate how much the input signal is corrupted by the circuit's noise. Similar to the device noise analysis, the offset voltage for each delay stage is referred back to the input of that stage and is represented by a voltage source, $V_{\rm OS,in}$. The same analysis proposed in [28] can then be applied to analyze the VCO phase noise due to the offset.

V. PLL Jitter Analysis

Due to their desirable features (e.g., not exhibiting any false lock, having a fast acquisition-time, and retaining a zero-phase offset in the lock condition), charge-pump PLLs, shown in Fig. 1, have found widespread use in frequency synthesis and timing recovery applications. The output voltage of the sequential PFD can be expressed as a linear function of the phase difference. The output voltage of the PFD acts like a control voltage for the switched current sources of the charge pump circuit. Finally, the transfer function of the second-order PLL incorporating a simple *RC* circuit as the LPF is easily obtained. For the related formulations and derivations see [19].

A general noise analysis of the PLL must be carried out using the nonlinear stochastic modeling of the PLL and by solving the Fokker–Plank characteristic stochastic differential equations. In a robust PLL circuit with a larger than required lock-range, the VCO phase noise induced by substrate and P/G noise generates the timing jitter at the PLL output without unlocking the PLL loop. Therefore, the PLL timing jitter in response to the VCO phase noise is obtained under the locked condition. The closed-loop PLL system is a linear feedback system under the locked condition and the PSD of the output is related to the spectral density of the VCO phase variations by the squared magnitude of the closed-loop transfer function

$$S_{\Phi_{\rm PLL}}(\omega) = \left|H_{\rm PLL}(\omega)\right|^2 S_{\Phi_{\rm VCO}}(\omega) = \left|\frac{1}{1+H_{\rm LP}(\omega)\left(\frac{I_{\rm PD}K_{\rm VCO}}{j2\pi\omega M}\right)}\right|^2 S_{\Phi_{\rm VCO}}(\omega) \quad (26)$$

where $H_{\rm LP}(\omega)$ is the loop filter, $I_{\rm PD}$ is the constant current source in the charge-pump circuit, $K_{\rm VCO}$ is the VCO gain, and M represents the frequency division factor, as also shown in Fig. 1. $S_{\Phi_{\rm VCO}}(\omega)$ is the PSD of the excess phase induced by substrate noise.

The PLL phase noise and timing jitter due to substrate noise are derived using (6), (25), and (26). For a second-order PLL circuit incorporating the first-order series RC circuit ($R_P - C_P$) as the loop-filter, and depending on the PLL circuit parameters, the closed-form expressions can be in one of the two possible following forms (the critically damped response is derived as a special case of the underdamped response):

$$\tilde{S}_{\Phi_{\rm PLL}}(\omega) = \overline{A^2_{\rm sub}}\frac{K^2_{\rm VCO,noise}}{p_2^2-p_1^2} \times\left(\frac{p_2^2}{\omega^2+p_2^2}-\frac{p_1^2}{\omega^2+p_1^2}\right) \text{ Overdamped} \quad (27)$$

$$\tilde{S}_{\Phi_{\rm PLL}}(\omega) = \overline{A^2_{\rm sub}}K^2_{\rm VCO,noise} \times\left(\frac{\omega}{\omega^2+|p_1|^2}\right)^2 \text{ Underdamped} \quad (28)$$

where $\overline{A^2_{\rm sub}}$ represents the total average noise power of substrate noise. In practice, the number of adjacent switching circuits is uncorrelated to the number of adjacent switching circuits in another location inside the chip. Therefore, the random amplitude of the noise spikes in (2), $A_{{\rm sub},N(P)}$, can be modeled as white noise process, which simplifies the noise calculation.

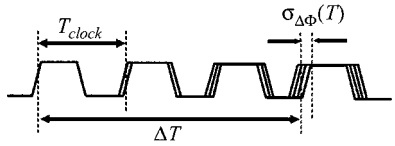

Fig. 14. Definition of the accumulated jitter.

Moreover, p_1 and p_2 are the closed-loop poles of the second-order charge-pump PLL circuit [roots of Laplace transform of the denominator in (26)]. The closed-loop poles of the PLL circuit will appear as a complex conjugate pair (i.e., $p_1 = p_2^*$) if the output phase exhibits an underdamped transient response. The poles lie on the negative real axis for an overdamped transient response (i.e., $p_1, p_2 \in \Re^-$, $p_2 > p_1$). Equations (27) and (28) state that the random variations in the zero-crossing time instants of the PLL output signal have a $1/f^2$ characteristic, therefore the error will have a spectrum that appears as a skirt on the spectral line of the fundamental frequency component.

In general, the timing jitter of the PLL is defined as [10], [14]

$$\sigma^2_{\Delta\Phi}(\Delta T) = \frac{2}{4\pi^2 f_0^2}\left[R_{\Phi_{\rm PLL}}(0) - R_{\Phi_{\rm PLL}}(\Delta T)\right] \quad (29)$$

where ΔT is the delay from the reference edge, f_0 is the synthesized output frequency of the PLL circuit, and $R_{\Phi_{\rm PLL}}(\Delta T)$ represents the autocorrelation of the PLL excess phase. This definition is in accordance to the procedure taken during the actual measurements of the PLL timing jitter, where the synthesized PLL signal is used as both the trigger and the input to digital oscilloscope or a communications signal analyzer. The oscilloscope compares the phase difference between the phase transitions in the clock waveform, separated by an interval ΔT from the reference edge (cf. Fig. 14). The oscilloscope, in fact, measures the variance of the zero-crossings.

The timing jitter is thus equal to

$$\sigma^2_{\Delta\Phi}(\Delta T) = \frac{\overline{A^2_{\rm sub}}}{4\pi^2 f_0^2}\left(\frac{K^2_{\rm VCO,noise}}{p_2^2-p_1^2}\right) \times\left[p_2\left(1-e^{-p_2|\Delta T|}\right) - p_1\left(1-e^{-p_1|\Delta T|}\right)\right] \text{ Overdamped} \quad (30)$$

$$\sigma^2_{\Delta\Phi}(\Delta T) = \frac{\overline{A^2_{\rm sub}}}{8\pi^2 f_0^2}\cdot\frac{K^2_{\rm VCO,noise}}{|p_1|} \times\left[1-(1-|p_1||\Delta T|) \times e^{-|p_1||\Delta T|}\right] \text{ Underdamped.} \quad (31)$$

VI. Simulation Results

A complete PLL clock generator circuit similar to the one proposed in [18] was designed in a 0.25-μm standard CMOS process. The PLL operates with a lock range from 50 MHz up to 500 MHz. a charge-pump PLL circuit is .

To experimentally emulate the switching of digital circuits and to generate the substrate noise caused by logic switching, 40 tapered inverters driving 1 pF capacitors were placed around the PLL clock circuit [cf. Fig. 4(a)]. To account for the randomness of the switching activity of digital circuits, the input signals

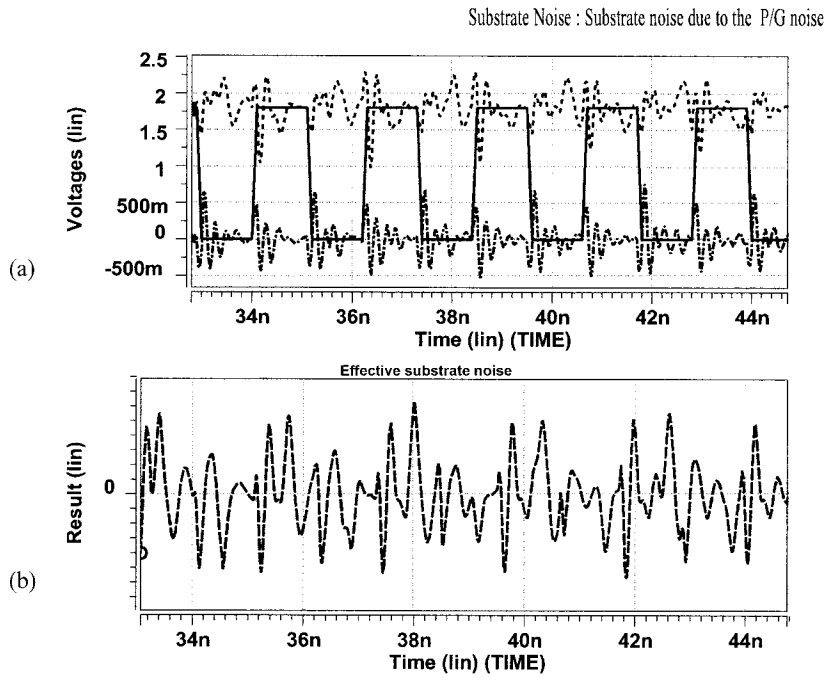

Fig. 15. (a) P/G noise due to simultaneous switching of the output buffers. (b) Effective substrate noise injected by the fluctuations of power-supply and ground lines.

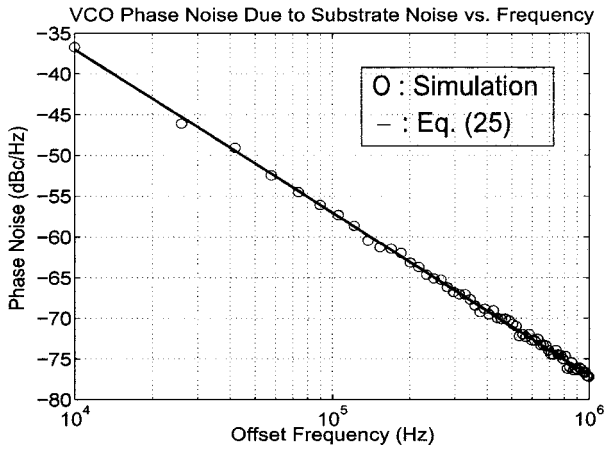

Fig. 16. Comparison between the phase noise of the designed VCO obtained using simulation and the one using (25).

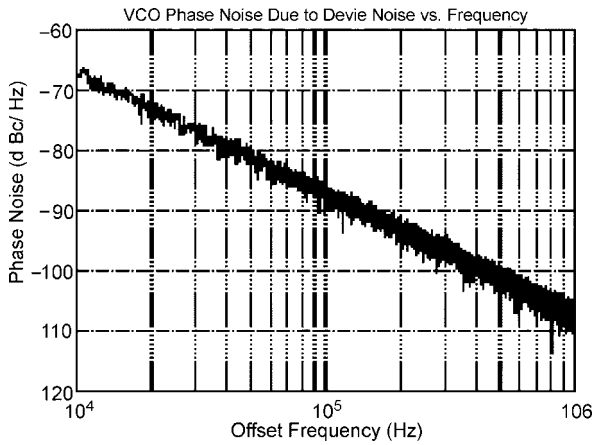

Fig. 17. VCO phase noise due to the device noise and device mismatch.

to the tapered buffers were generated by a pseudo-random generator with a Gaussian distribution. The circuit was laid out in a low epi process. Post-layout simulations were carried out to account for the metal and interconnect parasitics. Fig. 15(a) shows simulated P/G noise resulting from the simultaneous switching of tapered buffers. Fig. 15(b) depicts substrate noise injected by the signal fluctuations on the power-supply and ground lines.

To carry out the phase and jitter simulation and verify the analytical models developed in this paper, the average energy of substrate noise per cycle and the time at which substrate noise reaches its maximum were calculated. The noise information was then used to calculate the VCO phase noise and the PLL jitter using the proposed analytical models. Results of the calculation were compared with those obtained by the direct use of HSPICE simulation of the PLL circuit.

First, the noise spectra of the composing VCO circuit in the presence of substrate noise injection was obtained. Fig. 16 indicates the phase noise (in dBc/Hz) of the designed ring VCO calculated, once using the simulation; and then using (25). A comparison between the simulation and (25) reveals that the model accurately follows the simulation results over the frequency offset range of [10 kHz, 1 MHz]. Substrate and P/G noise constituted the major contributing components to the VCO phase noise. This was verified by simulating the VCO phase noise while all the surrounding buffers being quiet. Therefore, device mismatch and intrinsic device noise sources were the only noise sources that contributed to the VCO phase noise. Fig. 17 shows the result of this simulation. Comparing Fig. 16 with Fig. 17, the VCO phase noise due to the P/G and substrate noise is approximately 40 dB larger than that due to the device mismatch and device noise sources.

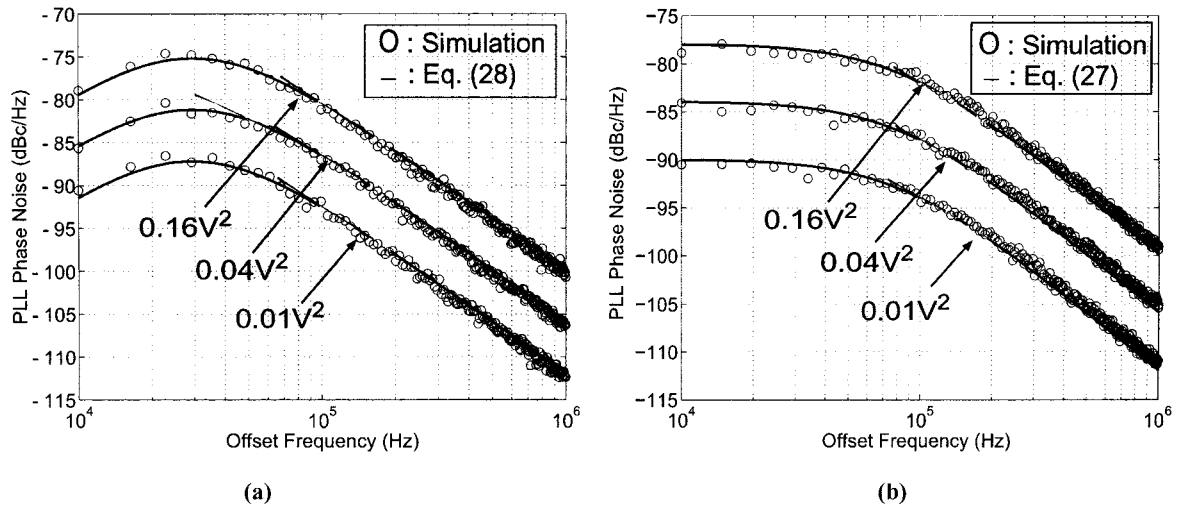

Fig. 18. Phase noise of the PLL output phase versus frequency. (a) Underdamped. (b) Overdamped.

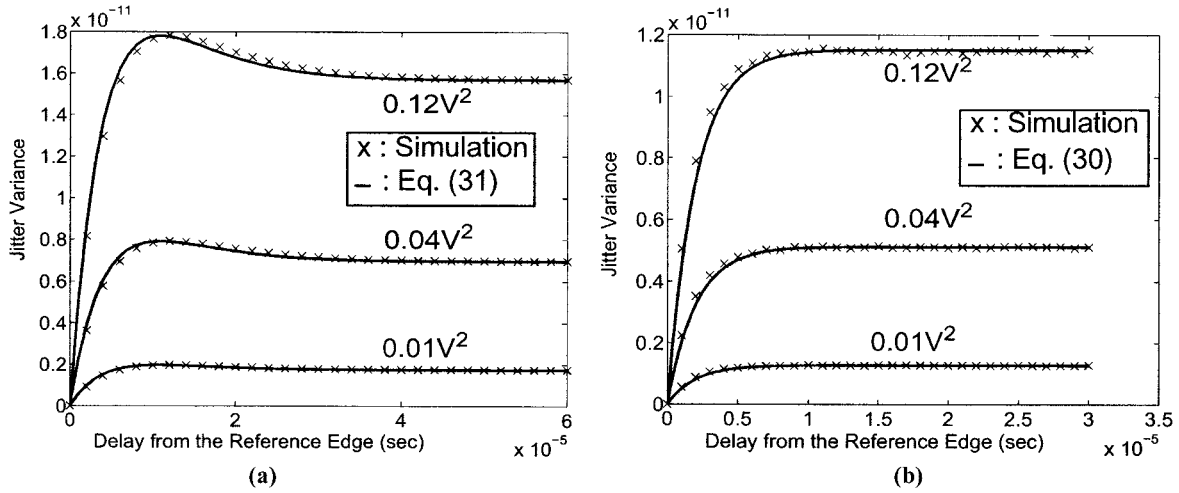

Fig. 19. Jitter variance of the PLL output phase versus the delay with respect to the reference edge. (a) Underdamped. (b) Overdamped.

The second experiment involves the phase noise of the PLL circuit for two cases of an underdamped response and having an overdamped response. The overdamped and underdamped cases were achieved by varying the damping ratio of the loop transfer function using two different values for the resistor of the loop filter.

Fig. 18(a) depicts the PLL phase noise versus frequency for the underdamped response. The phase noise was simulated under three different substrate noise couplings with different average powers. The proposed analytical model closely follows the simulation results over the frequency offset range and for different noise average power.

Fig. 18(b) demonstrates the PLL phase noise versus frequency for the overdamped response and under the three different substrate coupling waveforms with different average power. Once again, the analytical model accurately predicts the phase noise variations with respect to the frequency.

In the next simulation experiment, we simulated the PLL's jitter with respect to the delay from the reference edge, and compared the simulation result with the proposed analytical models. Performance comparison was made under three different substrate noise couplings. The jitter variance of the designed PLL circuit was calculated for two cases of an underdamped response and an overdamped response.

Fig. 19(a) shows the average power of the jitter (in V^2) versus delay for the underdamped response. The analytical model accurately follows the overshoot in the jitter profile that is predicted by simulation results for all three different substrate noise powers.

Fig. 19(b) shows the average power of the PLL jitter (in V^2) versus delay for the overdamped response. Once again, the analytical model is accurately predicting the phase noise variations with respect to the delay from the reference edge. As expected, the underdamped system shows a larger accumulated jitter.

VII. Conclusion

In this paper, an analysis of the PLL timing jitter due to substrate resulting from P/G noise and large-signal switching was presented. A general comprehensive stochastic model of the substrate and P/G noise sources in VLSI circuits was proposed. This was followed by calculation of the phase noise of the constituent VCO in terms of the statistical properties of substrate

and P/G noise. The PLL timing jitter was then predicted in response to the VCO phase noise. Our mathematical method was utilized to study the jitter-induced substrate and P/G noise in a CMOS PLL. A comparison between the results obtained by our mathematical model and those obtained by HSPICE simulation verified the accuracy of the predicted model.

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