8.4 A 1.8V Three-Stage 25GHz 3dB-BW Differential Non-Uniform Downsized Distributed Amplifier

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Distributed circuits using transmission lines (T-lines) or inductors exhibit high gain-bandwidth-products (GBW), as required by broadband communication systems. In this paper, the design of non-uniform downsized distributed amplifiers (DAs) is explored. Conventional DAs employ a topology in which inductors or T-lines separate the gain stages, yet the output currents from individual stages combine additively [1]. Major sources of performance degradation in any DA are the non-zero frequency-dependent loss of the inductors and the non-zero output conductance of the gain stages, which in turn decrease gain and BW. Previous works on distributed circuits do not consider the effect of inductor loss and output conductances of the constituent gain stages on the DA topology, leading us to an important question: Considering non-zero circuit losses, does a conventional DA with an optimum number of identical gain stages and segmental inductors achieve maximum GBW and better noise performance? To answer this question, mechanisms that affect gain and BW of conventional distributed circuits are studied, while non-zero losses are considered.

Equation (1) in Fig. 8.4.1 specifies the voltage-gain of an N-stage conventional differential DA shown in Fig. 8.4.1, and shows that the voltage transfer function of any conventional DA decreases exponentially with the attenuation of gate/drain lines [1]. The line attenuations, A_d and A_g, in the voltage transfer function of Eq. (1) vary with frequency. Consequently, to arrive at a DA with wider GBW, the variation of the line attenuation with frequency must be studied. Simulations of conventional DAs have shown that the gate and drain line attenuations become less frequency-dependent as the cutoff frequencies of the gate and drain lines, ω_{cg} and ω_{cd}, increase. More precisely, a linear increase in the attenuation of the line causes an exponential increase in the roll-off of the magnitude response (*cf.* Eq. (1)), which in turn causes an exponential decrease in BW. The bandwidth of the DA is determined by frequency variations of the lines' attenuations. On the other hand, the DC gain of a DA is linearly proportional to the transconductance of each gain stage, as indicated in Eq. (1). These observations constitute the cornerstone of a new topology for DAs that achieves a higher GBW than conventional distributed topologies. Because the bandwidth of the amplifier exponentially increases with a linear increase of the cut-off frequency of the line, downsizing the inductance of the line and the device size of each constituent gain stage will exponentially increase BW, while linearly decreasing DC gain. However, the first few stages of a DA contribute more to the overall signal amplification, because the incoming signals to the first stages have higher amplitude and average signal power than the signals traveling down to the last gain stages. This understanding guides us to a non-uniform differential DA, shown in Fig. 8.4.2, where the gain stages and inductors are progressively downsized toward the load termination with a constant tapering factor, K. This obviously means that g_m and parasitic capacitances of each transistor within each cell become $1/K^{th}$ of those of the transistor in the previous cell. The inter-stage inductor of each stage is also scaled down considering the notion that each inter-stage inductor is comprised of two series inductors, as also illustrated in Fig. 8.4.2. One inductor belongs to the T-section of the previous stage, and another one (whose value is $1/K^{th}$ of that of the previous stage) belongs to the T-section of the next stage. To attain a zero reflection from each tap-point, the characteristic impedances of all the artificial LC line segments, Z_{0k} for $1 \le k \le N$, are made identical. In the circuit of Fig. 8.4.2, each differential stage toward the load terminal is progressively downsized with a scaling factor of K while keeping the characteristic impedance of each LC section constant to achieve maximum power transfer toward the load. Each differential-pair is neutralized using a pair of cross-connected capacitors, C_D, as indicated in Fig. 8.4.1. These capacitors are realized using MOS devices whose drain and source are short-circuited. They are also scaled down with the same scaling factor, K. A fully differential architecture significantly reduces the sensitivity of the amplifier to substrate and P/G noise appearing as common-mode fluctuations. Moreover, progressive downsizing of the distributed circuit in Fig. 8.4.2 minimizes the input-referred noise, and hence the overall NF of the circuit, because it broadens the GBW of the DA.

A 3-stage fully differential non-uniform downsized DA with a scaling factor of 1.5 is fabricated in a sbc18 SiGe process provided by Jazz Semiconductor, where only CMOS transistors are employed in the design. A 1.8V supply voltage is used in the design. The 1.8V power supply draws a DC current of 30mA.

A complete set of s-parameter measurements of the circuit are carried out. Of particular interest is the measurement of differential-mode s-parameters. Figure 8.4.3 shows the differential forward gain s_{DD21}, and the circuit NF. The proposed circuit exhibited a flat gain of +7.8dB±1.3dB for frequencies up to 17.5GHz. Using linear extrapolation, the 3-dB BW is approximately 25GHz, which is beyond the measurement capability of the VNA. The NF measured by an HP8970S varied from 4.8dB to 7dB over the 20GHz BW. Figure 8.4.3 shows differential-mode reverse isolation, s_{DD12}, and the input and output return losses, s_{DD11} and s_{DD22}, respectively. s_{DD12} is less than -20dB, and s_{DD11} and s_{DD22} are less than -10dBm. The linearity and third-order intercept measurements are performed using the Agilent 8565EC spectrum analyzer. The measured input-referred 1dB compression-point at the input frequency of 12GHz is 4.2dBm. The result from the two-tone test measurement at 12GHz is shown in Fig. 8.4.5. The proposed DA circuit exhibited an IIP3 of +4.7dBm. Figure 8.4.7 compares the performance of the non-uniform DA circuit with some other previously published works. [5] achieves a 35GHz BW while dissipating more power and occupying more area than the proposed circuit. Figure 8.4.6 shows the chip micrograph. The circuit occupies a total area of 1.025x1.29mm^2 including the pad ring. To minimize the parasitic effects of chip-board interface, the chip is thus solder bumped, and flipped on the board. Dummy fill shapes have blocked parts of the circuit. The layout of the circuit is included for a better clarity.

Acknowledgement:
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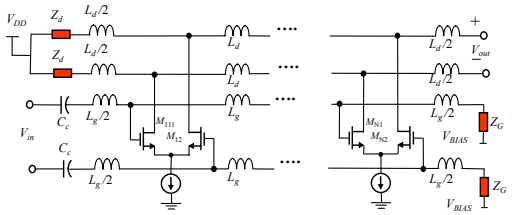
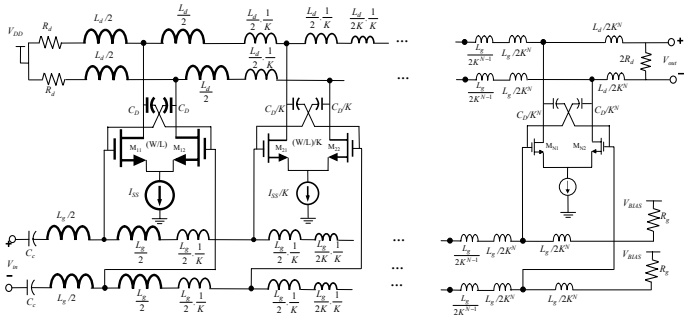
References:
[1] T. Y. Wong, Fundamentals of Distributed Amplification, Norwood, MA: Artech House, 1993.
[2] T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, 2nd ed., 2004.
[3] B. M. Ballweber et al., "A Fully Integrated 0.5-5.5GHz CMOS Distributed Amplifier," *IEEE J. Solid-State Circuits,* vol. 35, no. 2, pp. 231-239, Feb., 2000.
[4] H.-T. Ahn et al., "A 0.5-8.5GHz Fully Differential CMOS Distributed Amplifier," *IEEE J. Solid-State Circuits*, vol. 37, pp. 985-993, Aug., 2002.
[5] H. Shigematsu et al., "40Gb/s CMOS Distributed Amplifier for Fiber-Optic Communication Systems," *ISSCC Dig. Tech. Papers*, pp. 476-487, Feb., 2004.
[6] R. Liu et al., "A 0.6-22-GHz Broadband CMOS Distributed Amplifier," et al., *RFIC Symposium*, pp. 103-106, June, 2003.



$$(1)\qquad |A_v| = \frac{g_m (R_{0d} R_{0g})^{\frac{1}{2}} \sinh[\,0.5N(A_d - A_g)]e^{-N(A_d+A_g)/2}}{2[1-(\frac{\omega}{\omega_c})]^{1/2} \sinh[\,0.5(A_d - A_g)]}$$

g_m :Device transconductance
N :Number of stages
R_{0g}, R_{0d} : Series loss of inductors, L_g and L_d
A_g, A_d :Line attenuations
ω_c :line cutoff frequency ($\omega_{cg} = \omega_{cd}$) $= \frac{2}{\sqrt{L_d C_d}} = \frac{2}{\sqrt{L_g C_g}}$

Figure 8.4.1: A conventional differential DA



N = number of stages = 3; V_{DD}=1.8V
$L_d = L_g$ = 363pH; $R_d = R_g$ = 50Ω; K = 1.5
W/L = 180µm/0.2µm
C_D are realized using an MOS device whose drain and source are short-circuited

Figure 8.4.2: The circuit schematic of the proposed non-uniform down-sized distributed amplifier

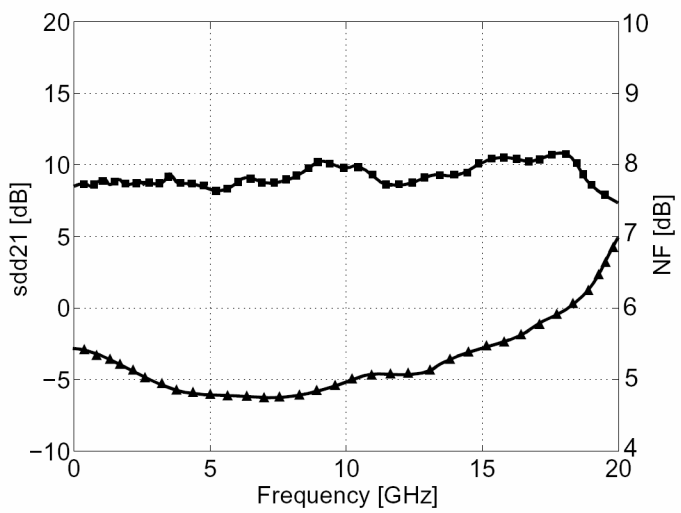


Figure 8.4.3: Measured forward gain and noise figure

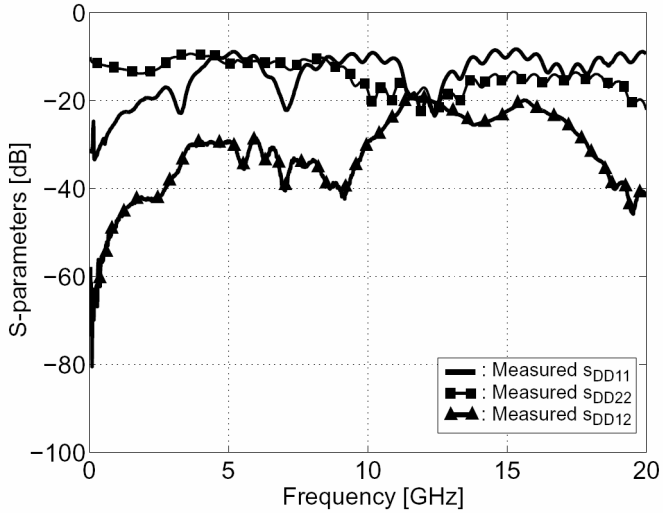


Figure 8.4.4: Measured input and output return losses, and reverse isolation

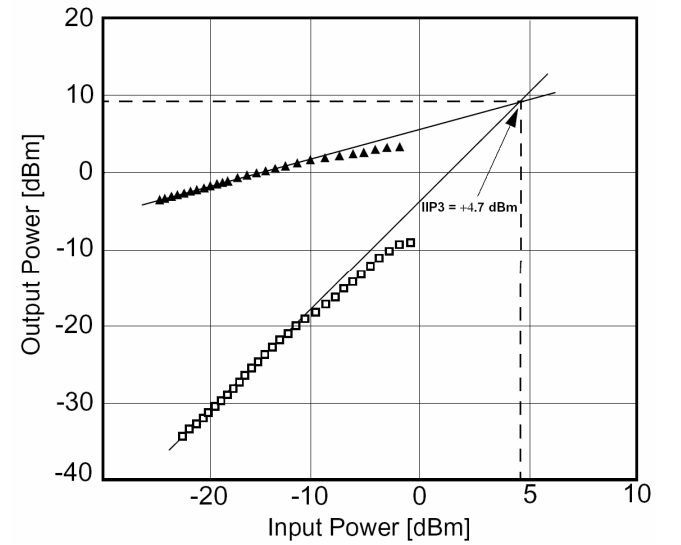


Figure 8.4.5: Measured two-tone test at 12GHz frequency

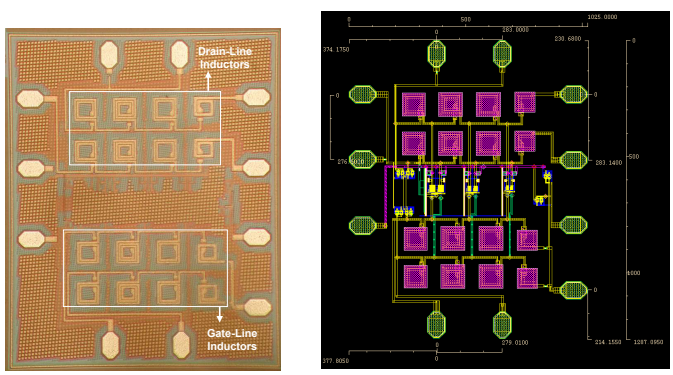


Figure 8.4.6: The die micrograph and the chip layout

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Ref	s_{21} (dB)	BW (GHz)	NF (dB)	IIP3 (dBm)	Power (mW)	V_{DD} (V)	Area (mm^2)	Technology
[3] (single-ended)	6.5 ±1.2 (0.5-4GHz)	0.5-5.5	5.4-8 (0.5-2GHz)	N/A	83.4	3	0.79	0.6μm standard CMOS
[4] (differential)	5.5± 1.5 (1.5-7.5GHz)	0.5-8.5	8.7-13 1-2GHz	N/A	216	3	1.3x2.2	0.6μm standard CMOS
[5] (single-ended)	4±1	35	N/A	N/A	140	1.8	1.1x3.0	0.18μm CMOS
[6] (single-ended)	7.3 ±0.8	0.6-22	4.3-6.1	N/A	52	1.3	0.9x1.5	0.18μm CMOS
This Work (differential)	7.8 ±1.3	25	4.8-7	4.7	54	1.8	1.025x1.29	0.18μm SiGe BiCMOS using only CMOS transistors

Figure 8.4.7: Performance comparison of DA circuits proposed in [3]-[6], and the proposed non-uniform downsized DA circuit

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