8.4 A 1.8V Three-Stage 25GHz 3dB-BW Differential Non-Uniform Downsized Distributed Amplifier

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Distributed circuits using transmission lines (T-lines) or induc-
tors exhibit high gain-bandwidth-products (GBW), as required by
broadband communication systems. In this paper, the design of
non-uniform downsized distributed amplifiers (DAs) is
explored. Conventional DAs employ a topology in which induc-
tors or T-lines separate the gain stages, yet the output currents
from individual stages combine additively [1]. Major sources of
performance degradation in any DA are the non-zero frequency-
dependent loss of the inductors and the non-zero output conduc-
tance of the gain stages, which in turn decrease gain and BW.

Previous works on distributed circuits do not consider the effect
of inductor loss and output conductances of the constituent gain
stages on the DA topology, leading us to an important question:
Considering non-zero circuit losses, does a conventional DA with
an optimum number of identical gain stages and segmental
inductors achieve maximum GBW and better noise performance?

Equation (1) in Fig. 8.4.1 specifies the voltage-gain of an N-stage
conventional differential DA shown in Fig. 8.4.1, and shows that
the voltage transfer function of any conventional DA decreases
exponentially with the attenuation of gate/drain lines [1]. The
line attenuations, $A_g$ and $A_p$, in the voltage transfer function of
Eq. (1) vary with frequency. Consequently, to arrive at a DA with
wider GBW, the variation of the line attenuation with frequency
must be studied. Simulations of conventional DAs have shown
that the gate and drain line attenuations become less frequency-
dependent as the cutoff frequencies of the gate and drain lines,
$\omega_o$ and $\omega_p$, increase. More precisely, a linear increase in the
attenuation of the line causes an exponential increase in the roll-
of the magnitude response (cf. Eq. (1)), which in turn causes an
exponential decrease in BW. The bandwidth of the DA is
determined by frequency variations of the lines’ attenuations.
On the other hand, the DC gain of a DA is linearly proportional to
the transconductance of each gain stage, as indicated in Eq. (1).
These observations constitute the cornerstone of a new topology
for DAs that achieves a higher GBW than conventional distrib-
uted topologies. Because the bandwidth of the amplifier exponen-
tially increases with a linear increase of the cut-off frequen-
cy of the line, downsizing the inductance of the line and the
device size of each constituent gain stage will exponentially
increase BW, while linearly decreasing DC gain. However, the
first few stages of a DA contribute more to the overall signal
amplification, because the incoming signals to the first stages
have higher amplitude and average signal power than the signals
traveling down to the last gain stages. This understanding

8.4.2

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Achieves a 35GHz BW while dissipating more power and occupying more
area than the proposed circuit. Figure 8.4.6 shows the chip micrograph.
The circuit occupies a total area of 1.025x1.29mm2 in the pad ring. To minimize the parasitic effects of chip-

board interface, the chip is thus solder bumped, and flipped on the board. Dummy fill shapes have blocked parts of the circuit. The layout of the circuit is included for a better clarity.

Acknowledgement:
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equipments, Sintegrity for designing the test board, and Jazz Semiconductor for providing the device data.

References:
Figure 8.4.1: A conventional differential DA

\[ A_i = \frac{g_m (R_{\text{in}} R_d)^{1/2} \sinh [0.5 N (A_i - A_j)] e^{-N(A_i + A_j)/2}}{2 \left[ 1 - \left( \frac{R_d}{R_g} \right)^{1/2} \sinh [0.5 (A_i - A_j)] \right]} \]

\( g_m \): Device transconductance
\( N \): Number of stages
\( R_{\text{in}}, R_d \): Series loss of inductors, \( L_g \) and \( L_d \)
\( A_i, A_j \): Line attenuations
\( \omega_c \): Line cutoff frequency \( (\omega_c = \omega_d) = \sqrt{\frac{1}{L_d C_d}} = \frac{2}{\sqrt{L_d C_d}} \)

Figure 8.4.2: The circuit schematic of the proposed non-uniform down-sized distributed amplifier

\( N = \text{number of stages} = 3; \ V_{\text{DD}} = 1.8 \text{V} \)
\( L_d = L_g = 363 \text{pH}; \ R_d = R_g = 50 \Omega; \ K = 1.5 \)
\( W/L = 180 \mu\text{m}/0.2 \mu\text{m} \)
\( C_d \) are realized using an MOS device whose drain and source are short-circuited

Figure 8.4.3: Measured forward gain and noise figure

Figure 8.4.4: Measured forward gain and reverse isolation

Figure 8.4.5: Measured two-tone test at 12GHz frequency

Figure 8.4.6: The die micrograph and the chip layout

Continued on Page 000
Figure 8.4.7: Performance comparison of DA circuits proposed in [3]-[6], and the proposed non-uniform downsized DA circuit

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<th>Ref</th>
<th>$v_{ip}$ (dB)</th>
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<th>NF (dB)</th>
<th>$I_{DS}$ (mA)</th>
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<th>$V_{DD}$ (V)</th>
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0.18µm SG4 BiCMOS using only CMOS transistors