

A Novel Ultra High-Speed Flip-Flop-Based Frequency Divider

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Abstract—Frequency dividers play an important role in high-speed communications systems. In particular, optical communication circuits demand frequency dividers capable of operating well above 10 GHz. This paper presents a high-speed flip-flop-based frequency divider incorporating a new high-speed latch topology, which provides satisfactory performance for frequencies up to 17 GHz. This circuit is designed and simulated in a standard 0.18 μm CMOS process.

1. Introduction

Frequency dividers are crucial circuits that are employed in PLLs and high-speed serializers/deserializers (serdes). Frequency dividers fall under three categories: (1) flip-flop-based frequency dividers [1], (2) injection-locked frequency dividers [2], and (3) regenerative frequency dividers [3], [4], [5].

Injection-locked frequency dividers employ an oscillator whose center frequency is locked to a harmonic of the incoming signal frequency. The input signal is injected through a voltage node of the oscillator. While achieving low-power operation, injection-locked frequency dividers exhibit a narrow lock-range.

Regenerative frequency dividers, first introduced in [3], are realized by placing a mixer and a low-pass filter in a closed-loop feedback. A regenerative frequency divider exhibits a wider lock range at very high frequencies compared to an injection-locked counterpart, but utilizes many passive components in the process. Since frequency dividers are ubiquitous in modern high-speed systems, the excessive use of passive components is a disadvantage from overall chip-area and circuit matching considerations.

The flip-flop-based frequency dividers are comprised of two D-latches in cascade, and in a negative feedback configuration [1]. The digital operation of this type of dividers provides the advantage of suppressing the sensitivity to waveform distortions. Furthermore, the flip-flop-based dividers achieve a wide bandwidth than other types of frequency dividers at low-to-medium range of frequencies. This approach also makes the signal levels compatible with the rest of the CML circuit blocks. High-speed flip-flop based frequency dividers are typically implemented using the current-mode-logic (CML) latches. Large frequency ranges (GHz) are not therefore uncommon in flip-flop-based frequency dividers that use CML logic style. However, a major disadvantage associated with conventional frequency dividers using CML style stems from the large load capacitances seen by the circuit blocks, which limit the maximum frequency of operation and fan-out capabilities.

This work explores the extension of flip-flop-based dividers to higher frequencies by introducing novel high-speed latch topologies. The paper starts with Section 2 that includes a description of flip-flop-based frequency dividers followed by a detailed discussion of the proposed latch design in Section 3. Section 4 provides simulation results of the proposed latch and frequency divider. Finally, Section 5 presents concluding remarks.

2. Circuit Architecture

This paper uses the flip-flop-based circuit architecture to realize the frequency divider, as shown in Fig 1. This architecture is primarily a master-slave flip-flop with a negative feedback. This circuit works by continually toggling the output state after every clock cycle. The mechanism effectively causes the output to toggle between one and zero at a rate half that of the input clock. Thus frequency division is achieved. Fig. 2 shows the clock pulses and the output from each of the latches explaining the circuit action.

The basic enabling circuit block in this topology is the D-latch. A high-speed latch automatically results in a high-speed frequency divider. As a result, Section 3 is dedicated to high-speed latch design.

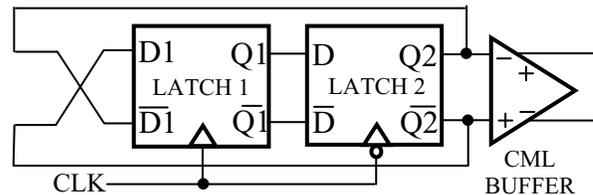


Fig. 1. Flip-flop based divider topology

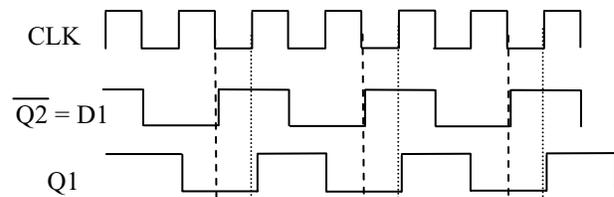


Fig. 2. Flip-flop based divider operation

3. Latch Design

This section is dedicated to the design of high-speed latch circuit. The proposed latch topologies will also be discussed in this section.

3.1. Conventional latch

High-speed latches are designed using current-mode logic (CML) circuits. Shown in Fig. 3 is the conventional CML latch topology.

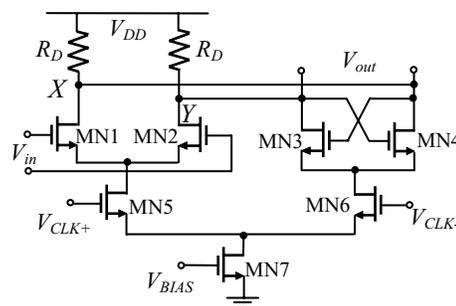


Fig. 3. Conventional latch circuit

The track and latch modes are determined by the clock signal input to a second differential pair, MN5 and MN6. When the signal V_{CLK} is "HIGH", the circuit operates in the tracking mode, where the tail current from MN7 flows entirely to the tracking circuit, MN1 and MN2, thereby allowing V_{OUT} to track V_{in} . In the latch-mode, the signal V_{CLK} is held low and the tracking stage is disabled, whereas the latch pair is enabled storing the logic state at the output.

Similar to CML buffers, a CML latch operates with relatively small voltage swings, which is $2V_{THN}$ peak-to-peak differential-mode (V_{THN} is the NMOS threshold voltage) [6]. However, there are several shortcomings involved in the design of the regenerative latch in Fig. 3, that lead to a complete operation failure at very high speed data-rates ($> 10\text{Gbit/sec}$).

The primary limitation is that a single tail current is used for both tracking and latch circuits. Consequently, the bias operations of tracking and latch circuits are tightly related. This severely limits the allowable transistor sizes for a reliable latch operation. At ultra high-speed data-rates, the parasitic capacitances of transistors, MN1 and MN2, degrade the required minimum small-signal gain for a proper tracking operation. Therefore, the tail current must be sufficiently high to achieve a wider range of linearity and a larger transconductance (g_m). However, a larger transconductance means larger device sizes, and therefore, larger parasitic capacitances. Parasitic capacitances of MN1 and MN2 directly contribute on the latch delay. On the other hand, the latch circuit does not need a large bias current for ultra high-frequency operation.

3.2. New topologies for high-speed latch

To address the aforementioned problems, the regenerative CML latch is modified so that the latch circuit and the tracking circuit use two distinct tail currents. This gives an additional design option to optimize the delay as well as the regenerative gain. Fig. 4 shows the new CML latch circuit.

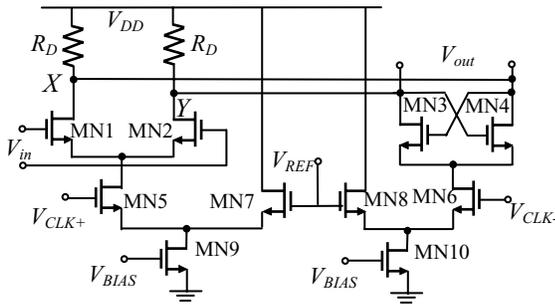


Fig. 4. Modified latch circuit

As observed in Fig. 4, the tracking stage and the latch stage are now separately optimized for a correct latch operation at ultra high-speed. Note that it is important for the cross coupled pair transistors MN3-MN4 to have high gain to reduce the latch settle time, which occurs through positive feedback. This is obviously achieved by up-sizing each transistor in the cross-coupled pair (MN3 and MN4 in Fig. 4). However the current drive capability of the CML latch circuit is still limited as the large cross-coupled pair transistors introduce larger gate capacitance when being turned on for latch action. Therefore, the CML latch has to be followed by another CML buffer to recover the logic level.

There is another underlying problem that causes a speed limitation on the proposed circuit as well as the conventional counterpart. During each transition from the tracking mode (when V_{CLK} is "HIGH") to the latching mode (when V_{CLK} is "LOW"), the current tail of the cross-coupled pair must first recharge the capacitances of the cross-coupled pair as it starts drawing current from the output nodes, X and Y, and changing the logic state. This will increase the minimum achievable clock period at which the latch circuit works properly.

An alternative to the proposed circuit of Fig. 4 is depicted in Fig. 5, where the latch cross-coupled pair, MN3 and MN4, always draws current from the nodes X, Y and there is no need for the charge to be built up during the latching phase. In addition, there are several other advantages associated with the circuit of Fig. 5.

Firstly, the new CML latch circuit does not suffer from the current spiking seen at the drain of the clock transistors. This phenomenon becomes clear by studying the circuit in the tracking mode when the input signal V_{CLK} is "HIGH". During the tracking interval, transistor MN8 is switched on drawing a portion of the tail current and reducing the current spikes. On the other hand, the cross-coupled pair MN3-MN4 is always enabled; hence no current spike occurs during the transition from tracking to latching mode.

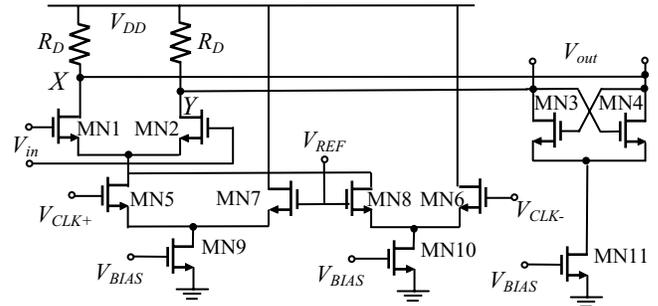


Fig. 5. Novel latch circuit

Secondly, an enabled cross-coupled pair during the tracking mode directly contributes to smaller rise and fall times for the output voltages at nodes X and Y. The reason is that cross-coupled pair exhibits a negative resistance that lowers the equivalent resistance at each node X and Y for a fixed output voltage swing, thereby decreasing rise and fall times of the output voltages.

The new latch circuit, however, consumes more power than the circuits shown in Figs. 3 and 4 because of an additional current tail. The above latch topologies were first analyzed as double edge-triggered flip-flops without feedback and later incorporated as frequency dividers using the circuit architecture in Fig 1. Improvements in rise-time and drive capability of the standalone flip-flop output at high frequencies are key enablers of frequency division by the flip-flop using the latches at those frequencies.

4. Simulation Results and Discussion

4.1. Latch operation

The performance comparison of the latch circuits are made by separately incorporating latches from Figs 3 and 5 in an ultra high-speed positive-edge triggered D-flip-flop that retimes the input data with a rate of 20 Gbit/sec using a half-rate clock signal at 10 GHz that is locked to the input data. To perform a meaningful and sound comparison, all latches are designed to be identical in terms of the current levels, transistor sizes and drain resistors. Figs. 6 and 7 demonstrate outputs of flip-flop circuits consisting of latch circuits of Figs. 3 and 5 at 20 GHz data-rate, respectively. The output nodes of the flip-flop made of conventional CML latches exhibits large ringing that can lead operation failure. The ringing is largely reduced at the output voltages of the flip-flop consisting of the latch shown in Fig. 5. Besides, the output signal transients are smaller compared to those in the conventional flip-flop circuit. The proposed CML latch circuit in Fig. 5 has a superior performance compared to the one shown in Fig. 3 for the input data-rate.

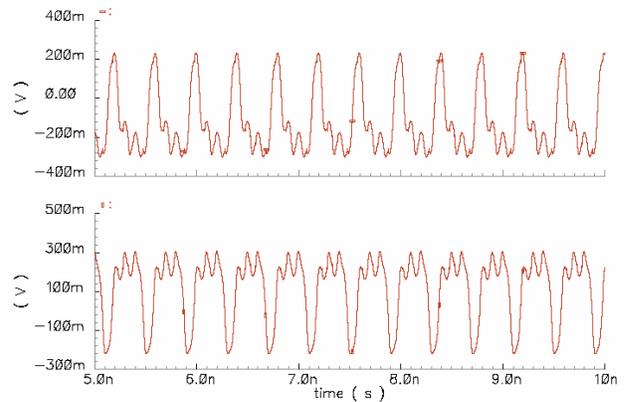


Fig. 6. Output from conventional latch based flip-flop

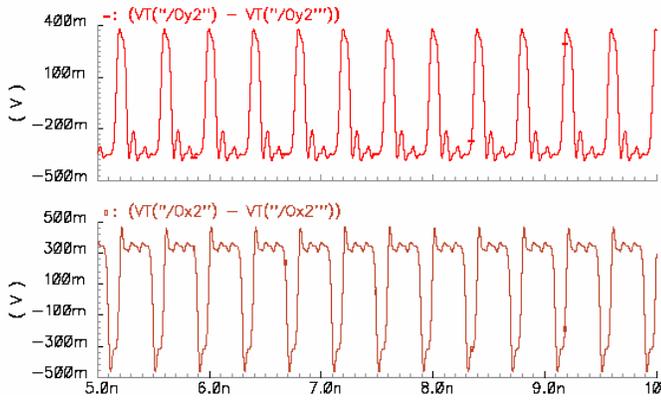


Fig. 7. Output from novel latch based flip-flop

A commonly used figure of merit for visualizing the non-idealities of the latch circuits is to use a pseudo-random bit sequence (PRBS) at the inputs of the latch circuits to emulate the actual data pattern in the data communications transceiver, and obtaining the eye diagram. A random data sequence of 64-bit long is used as input to latch circuits in Figs. 3 and 5. Figs. 8 and 9 indicate the eye diagrams for the circuits of Figs. 3 and 5, respectively. From the eye diagrams, one can clearly find out that the proposed latch circuit of Fig. 5 exhibits a faster slew-rate compared to the conventional latch shown in Fig. 3.

As illustrated in Section 3, the latch circuit in Fig. 5 also diminishes the current spikes at the tail current. This observation is verified by comparing the current waveforms of Figs. 10 and 11 for the latch circuits shown in Figs. 3 and 5, respectively.

While the tail currents MN5-MN6 of the latch circuit of Fig. 3 exhibit spikes, the tail currents MN5 –MN6 of the latch circuit in Fig. 5 do not show any spikes.

4.2. Frequency divider

To compare the performance of frequency dividers incorporating the latch circuits in Figs. 3 and 5, input clock signals at different frequencies and amplitudes are applied to these frequency dividers and the output waveforms recorded for frequency division. This experiment leads to the sensitivity curves shown in Fig 12. According to Fig. 12, the frequency divider utilizing the circuit of Fig. 5 exhibits a wider frequency range of up to 17 GHz compared to a 14 GHz range for the frequency divider incorporating the circuit of Fig. 3. Another underlying advantage of the novel frequency divider compared to the conventional counterpart is well understood by studying the dynamic characteristics of the flip-flop-based frequency divider, described below.

The sensitivity curves show a minimum differential voltage needed for frequency division at a certain intermediate frequency. It has been shown in [7] that this phenomenon is due to the instability of the circuit at certain frequencies due to the pole introduced by the cross-coupled pair. This leads to self-oscillation of the circuit at this frequency, and the circuit requires small differential amplitudes for oscillation. Fig 14 shows the cross-coupled pair highlighting the elements contributing to self-oscillation. The frequency of self-oscillation is given by $\omega \approx |g_m R - 1| / C_L R$. As explained in Section 3.2, to achieve a given rise and fall times, transistor sizes of the tracking circuit in Fig. 5 can be made smaller than those in Fig. 3, therefore, it becomes evident that the novel latch sees a much lower C_L than the conventional latch translating to a higher frequency of self-oscillation. The current tail feeding the cross-coupled pair can be used to achieve the desired g_m independent of optimal tracking operation of the first stage. As also mentioned in Section 3.2, the novel latch consumes more power than the conventional latch. To alleviate this problem, a frequency divider is designed using the novel latch as the first latch in Fig. 1, and a conventional latch as the

second one. The sensitivity curve using the hybrid latch is shown in Fig 12. It is evident that a compromise between power consumption and maximum frequency range could be achieved based on the application.

Fig. 13 shows the eye diagrams of the input and output clocks at the two extremes of the frequency range.

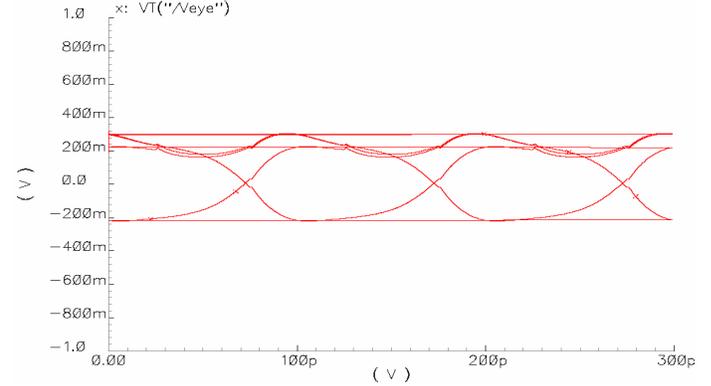


Fig. 8. Eye diagram from conventional latch based flip-flop

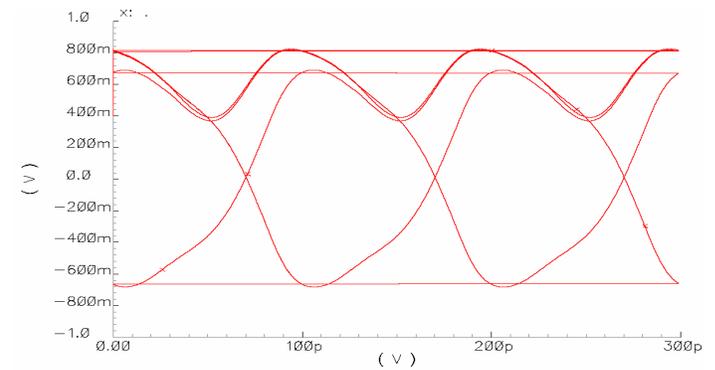


Fig. 9. Eye diagram from novel latch based flip-flop

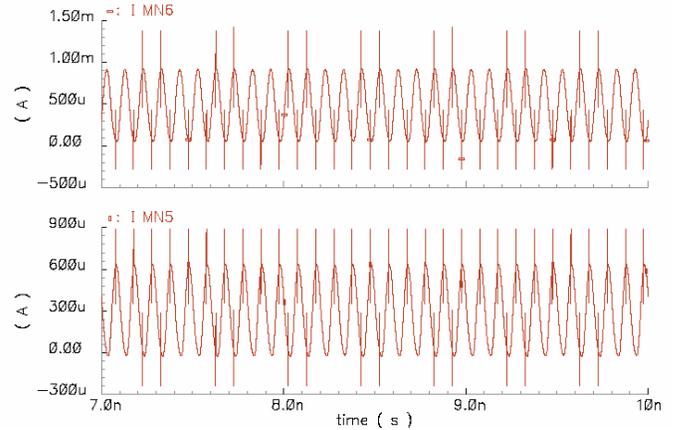


Fig. 10. Current spiking in conventional latch based flip-flop

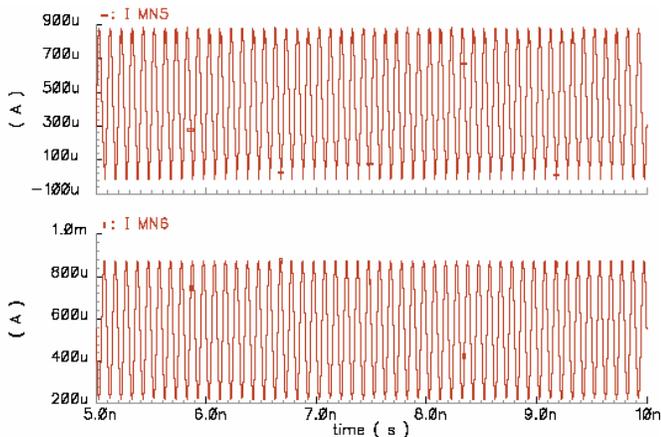


Fig. 11. No current spiking in novel latch based flip-flop

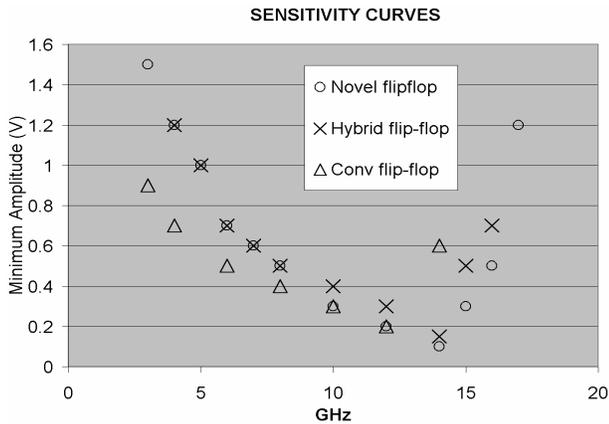


Fig. 12. Sensitivity curves of flip-flop based dividers

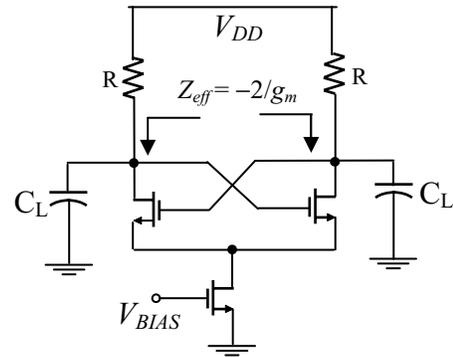


Fig. 14. Negative resistance in cross-coupled pair [7]

5. Conclusions

This paper demonstrated novel CMOS CML latch circuits functioning at multi-Gb/s speed that were directly used to realize ultra high-speed flip-flop-based frequency dividers. The novel frequency divider performed frequency division for frequencies up until 17 GHz without any shunt-peaking inductors. The power consumption of the novel frequency divider was higher than the conventional counterpart, which was alleviated by using a hybrid flip-flop.

6. Acknowledgement

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7. References

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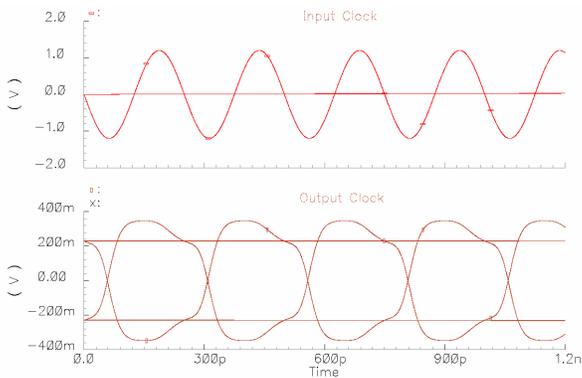


Fig. 13 a. Eye diagram of novel latch based divider at 4GHz

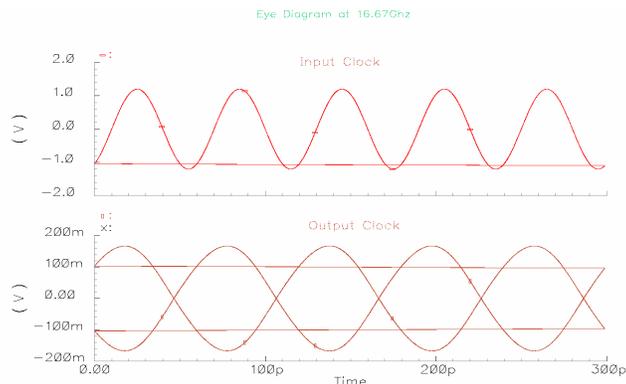


Fig. 13 b. Eye diagram of novel latch based divider at 16.7GHz