Design and Analysis of a Distributed Regenerative Frequency Divider Using a Distributed Mixer

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ABSTRACT

In this paper we present the design and analysis of a distributed regenerative frequency divider (DRFD) based on a novel distributed single-balanced mixer. Artificial transmission lines are incorporated in the distributed single balanced mixer to absorb the parasitic capacitances. The circuit is realized in a 0.18 μm standard CMOS process. It shows a division by two for an input frequency of 40 GHz, while consuming 10 mW from a 1.8-V supply.

1. INTRODUCTION

Frequency dividers are ubiquitous building blocks employed in a wide variety of important high-speed and radio-frequency (RF) integrated circuits, such as phase-locked loops (PLLs) and high-speed serializers/deserializers (SERDES). Introduced by Miller in 1939, a regenerative frequency divider is essentially a non-linear feedback circuit consisting of a mixer and a loop-filter, as shown in Figs. 1 (a) and (b). The steady-state operation of the circuit is straightforward. First, the output signal at frequency $\omega_{in}/2$ is mixed with the input signal at frequency ω_{in}. The mixer generates components at sum and difference frequencies $\omega_{in}/2$ and $3\omega_{in}/2$. The sum frequency component at $3\omega_{in}/2$ component is then filtered out by a low-pass or a band-pass filter. The difference frequency component $\omega_{in}/2$ is continuously regenerated inside the loop, hence the name "regenerative frequency divider".

In spite of having a simple steady-state operation, a regenerative frequency divider demonstrates a complicated startup and transient operations. [1],[2],[6] studied the transient behavior of a regenerative frequency divider, and showed that to establish a correct half-frequency regeneration, the loop gain at the half-frequency must be higher than unity, and the total loop phase at the half-frequency must be in intervals of $\pm\frac{\pi}{2}$ [1],[8].

The most important block in a regenerative frequency divider is the mixer. The aforementioned loop-gain condition for a regenerative frequency divider makes the active mixer (either single- or double-balanced) a proper choice for the divider realization [1], [3]. Conventional active mixers are, however, incapable of achieving sufficient phase-shift and conversion gain at very high-frequencies, demanding a new architecture for the constituent.

In this paper, we present the design and analysis of a novel frequency divider comprised of a distributed single-balanced mixer to achieve the division-by-2 of an input signal running at a 40 GHz frequency. The advantages of this distributed mixer are two-fold. Firstly, it exhibits a wideband conversion gain. Secondly, it introduces sufficient phase shift to satisfy the phase-shift requirement for a proper regenerative frequency division. The distributed mixer incorporates LC ladder circuits to realize the artificial transmission lines.

The paper is organized as follows: Section 2 illustrates the architecture of the proposed frequency divider, and presents a comprehensive analytical model for stable operation of the divider. Section 3 gives the simulation results. Finally, Section 4 provides the concluding remarks.

2. DISTRIBUTED FREQUENCY DIVIDER

There are two types of regenerative frequency dividers, as shown in Fig. 1, depending on which port of the mixer is utilized for the injection of the input signal.

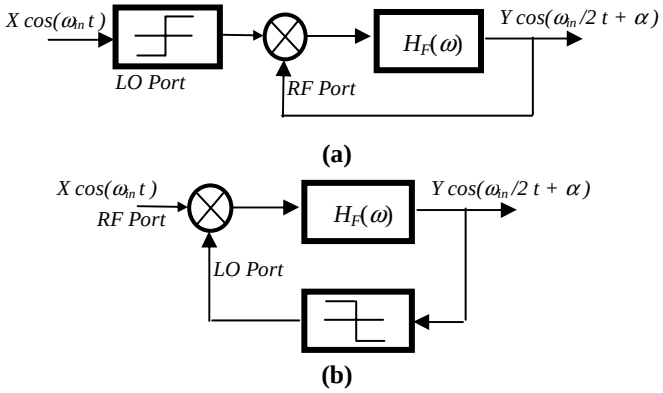

Fig. 1. Regenerative frequency divider (a) LO, and (b) RF port signal injected

In a distributed mixer the single balanced cells are distributed along the transmission lines. An example of a 2-stage distributed mixer is shown in Fig. 2. In the proposed frequency divider, the transmission lines are realized using LC ladder circuits[1]. Five distinct RF, LO, and IF artificial lines are used in the circuit, as shown in Fig. 2. Total gate and drain capacitances along with the inductors provide the artificial transmission lines.

In the current realization of the mixer, each cell is chosen to be a single-balanced mixer. However, other topologies of

[1] Another alternative is use on-chip micro-strip lines.

current commuting mixers, such as Gilbert-cell, can also be incorporated. The current tail transistors (M_{31}, and M_{32}) are all identically matched because of uniform transmission lines. The switching pair transistors have the same geometry. The output and input signals to each single-balanced cell are connected to the tap points of constituent artificial LC transmission lines. In [7], we prove that the phasor IF differential output voltage , V_{IF}, of an n-stage distributed mixer can be written as:

$$V_{IF} = \frac{n}{2} Z_0 g_{mRF} V_{RF}\, p_{11}(LO) \left| A(\omega) H_F(\omega) \right| e^{-j\, n\, \omega t_d + \angle A(\omega) + \angle H(\omega)} \qquad (1)$$

where n is the number of distributed stages, g_{mRF} is the transconductance of the tail transistor, and p_{11}(LO) is the first-order harmonic of the periodic instantaneous current gain of the switching pair [5]:

$$p_1(t) = \frac{g_{m1}(t) - g_{m2}(t)}{g_{m1}(t) + g_{m2}(t)} \qquad (2)$$

which is a function of LO signal amplitude and frequency, and $g_{m1,2}$ are the instantaneous transconductances of transistors in each switching pair in Fig. 2. t_d ($=\sqrt{LC}$) is the delay of each LC section in an artificial transmission line, which is assumed to be equal for RF, LO, and IF lines. $A(\omega)$ is frequency dependent part of the mixer frequency response, which represents the effect of existing dominant pole at each common source node P in Fig. 2. $H_F(\omega)$ is the loop filter frequency response (see Fig. 1).

We consider two systems in Figs. 1 (a), and (b) separately, to analyze the loop-gain criterion. As will be illustrated in Section 2.3 the phase criterion for both systems is the same. In other words the phase criterion is independent of where input signal is injected and is a function of total loop phase.

The attributes of the distributed mixer, including a wideband conversion gain, and a sufficient phase-shift, allow us to use a simple a first-order *RC* circuit as the loop-filter.

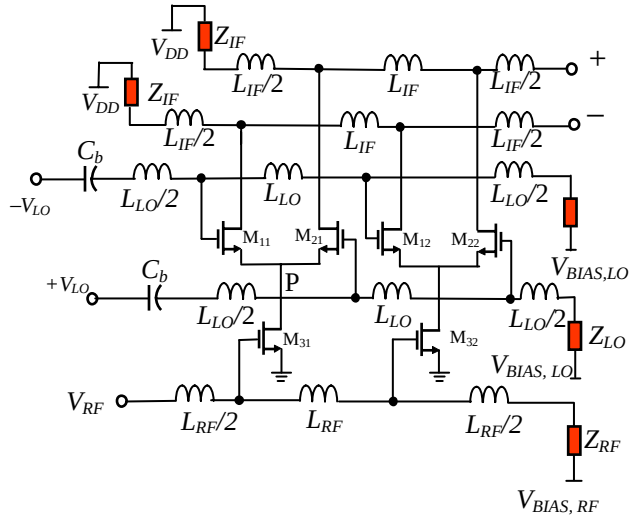

Fig. 2. Distributed single balanced mixer using in frequency divider

2.1. Input signal applied to the LO port

Consider the system in Fig. 1(a), where the input signal is applied to the RF port of distributed mixer in Fig. 2. The loop-gain criterion states that to have a regenerative frequency division, the loop-gain of the closed-loop frequency divider must be greater than unity, i.e.,

$$p_{11}(X) \geq \frac{2}{\frac{n}{2} Z_0 g_{mRF} \left| A(\omega_{in})\, H_F(\omega_{in}/2) \right|} \qquad (3)$$

where input signal with frequency of ω_{in} experiences $A(\omega)$ in its path to output, as shown in Fig. 2. Hence, it should be calculated at ω_{in}. For large enough X (input ampliude), p_{11} approaches $4/\pi$. Therefore, (3) becomes a simple design guideline to choose the bias current and size of tail transistor to achieve enough g_{mRF} to satisfy loop gain criterion. In other words it determines the minimum required gain of mixer, i.e.:

$$Mixer\_gain = \frac{2}{\pi} \frac{n}{2} Z_0\, g_{mRF} \geq \frac{1}{\left| A(\omega_{in})\, H_F(\omega_{in}/2) \right|} \qquad (4)$$

2.2. Input signal applied to the LO port

In this case the loop gain condition is(see Fig. 1(b)):

$$X \geq \frac{2Y}{\frac{n}{2} Z_0\, g_{mRF}\, p_{11}(Y) \left| A(\omega_{in})\, H_F(\omega_{in}/2) \right|} \qquad (5)$$

To calculate the minimum required input voltage to establish correct division, (5) should be examined at start up point when the output amplitude is almost zero. Hence it needs to calculate $p_{11}(Y)$ while Y approaches to zero. By substituting the instantaneous transconductance $g_{m1,2} = k(v_{gs}-V_t)$ in (2) we arrive at :

$$\lim_{Y \to 0} \frac{Y}{p_{11}(Y)} = \frac{1}{2\left(V_{BIAS,LO} - V_p - V_t\right)} \qquad (6)$$

where V_P and $V_{BIAS.LO}$ are bias voltages of node P and LO, respectively, as shown in Fig. 2. By substituting (6) in (5), the minimum input required voltage for correct division at the start up point becomes:

$$X_{\min} \geq \frac{4\left(V_{BISAS\ ,LO} - V_p - V_t\right)}{\frac{n}{2} Z_0\, g_{mRF} \left| A(\omega_{in})\, H_F(\omega_{in}/2) \right|} \qquad (7)$$

From (7) it is clear that if the number of stages in distributed mixer, n, increases the minimum required input level for correct division decreases.

The divider in Fig. 1(b) is similar to an injection locked frequency divider, then we may assume an input phasor of $I_{DC}+I_{RF}\, e^{j\omega t}$ and output phasor of $V_0\, e^{j(\omega/2\, t-\phi)}$, where I_{DC} is the bias current of tail transistors and I_{RF} is injected input current ($g_{mRF}V_{RF}$). It is supposed that in the steady-state the amplitude of output signal is large enough to cause $p_1(t)$ a square wave. Hence the loop gain condition can be written as: (8)

$$\frac{n}{2} Z_0\, g_{mRF} \left| A(\omega_{in})\, H_F(\omega_{in}/2) \right| \left| \frac{4}{\pi} I_{DC} e^{-j\phi} + \frac{4}{2\pi} I_{RF} e^{j\phi} - \frac{2}{6\pi} I_{RF} e^{-j2\phi} \right| \geq 1$$

In this case, when the input signal is applied to RF port of mixer, the general loop gain criterion in steady-stat operation can be written as: $k\,F(\omega)\,f(I_{RF}, I_{DC}, \phi) \geq 1$ (9)

where $F(\omega)$ is total frequency dependency due to loop filter, mixer, and transmission line frequency response. k is constant and f is function of input signal, bias current, and output phase, ϕ. The output amplitude does not appear in (9) because it is assumed that in steady-state operation output amplitude is large, hence $p_{11}(LO)$ approaches $4/\pi$ and becomes independent of LO amplitude. However at start up point, when output amplitude is zero, it is shown in (7) that loop gain condition is independent of output amplitude.

To examine the minimum required input at frequency offset of $\Delta\omega$ from ω_{in}, (8) should be solved numerically, which is plotted in Fig. 4, in contrast to simulation results, for 3 different tail bias currents of 2.8, 3.8, and 4.8 mA.

2.3. Phase Criterion

Both systems in Fig. 1 have the same steady state phase criterion for correct division operation [1],[2],[8]. Assuming $H_F(\omega)$ a first-order low-pass filter, the total frequency dependent phase of loop is:

$$\theta_{Loop}(\omega) = n\omega t_d + \tan^{-1}(\omega/\omega_p) + \tan^{-1}(\omega/\omega_F) \quad (10)$$

where ω_p and ω_F are the poles of $A(\omega)$ and $H_F(\omega)$,respectively. It is shown in [1],[8] that for stable operating division:

$$(2k\,\pi-\pi/2) < \theta_{Loop} < (2k\,\pi+\pi/2) \quad \text{k=integer} \quad (11)$$

By solving (11) there exist stable regions for correct division regarding to input frequency, ω_{in}. Increasing number of stages, n, leads to an increase in the slope of loop phase, $\Delta\theta_{Loop}/\Delta\omega$ in (10), hence reduces the width of stable regions regarding to input frequency.

Besides a change in ω_F due to process could increase the minimum required input level for correct operation, as shown in Fig. 6. It shows that for a 13% deviation in ω_F, divider needs more than 10dBm increase of input power for correct division.

Moreover variation in delay of each section of transmission lines, t_d, due to process variation could result in a deviation in output frequency from $\omega_{in}/2$, or an increase in minimum required input level for correct division. For example Simulation results, shown in Fig. 3, depicts that a variation of 5% in t_d results in a deviation of 0.75GHz in output frequency for a -30dBm 40GHz input frequency, but increasing input power to -4dBm forces the output frequency to 20 GHz. Here we calculate the required deviation in pole of loop filter, ω_F, to compensate the variation Δt_d of transmission line. To have a stable operation loop phase, θ_{LOOP}, should be equal for both cases, i.e.:

$$\theta_{LOOP}(t_d, \omega_{F1}) = \theta_{LOOP}(t_d + \Delta t_d, \omega_{F1} + \Delta\omega) \quad (12)$$

Substituting (10) in (12) and assuming that $n\omega\Delta t_d << 1$ and $\omega_{F1} = \omega_{in}/2$, we arrive at:

$$\Delta\omega \cong 2n\omega_{in}^2 \Delta t_d \quad (13)$$

In other words Δt_d causes a deviation in output frequency from $\omega_{in}/2$ or an increase in minimum required voltage for correct division.

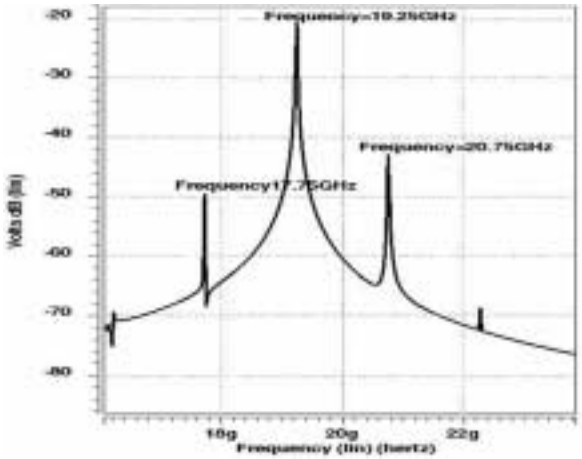

Fig. 3. Divider output Spectrum for a 40GHz input signal with $\Delta t_d/t_d$=5%

3.SIMULATION RESULTS

The frequency divider in Fig. 1(a) is realized using distributed single balanced mixer shown in Fig. 2, in 0.18-μm standard CMOS process. The inductors L_{RF}, L_{LO} and L_{IF} are 1nH. The termination impedances $Z_{RF,\,LO,\,IF}$ are 50 Ω. A simple RC low-pass filter with ω_{3dB} of 20 GHz is used as the loop filter, $H_F(\omega)$. The bias current I_{DC} is set 2.8, 3.8 and 4.8mA.

Fig. 4 shows the minimum input power required for different bias tail currents. The x-axis is the offset frequency, $\Delta\omega$, from 40GHz.

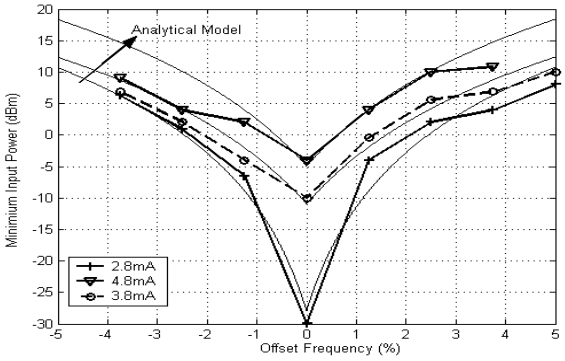

Fig. 4. Minimum required input vs. Offset frequency

Also the solid lines are the analytical model of minimum required input, from (8). The analytical model graphs are plotted numerically. There is a good agreement between the simulation results and analytical model from (8). Moreover it is clear form Fig. 4 that increasing the bias current requires more input power for correct division.

Fig. 5 shows the output power of divider regarding to offset frequency for different bias currents, I_{DC}. It shows that in the operating region the worst-case output power variation is less than 2.5dBm for I_{DC}=3.8mA.

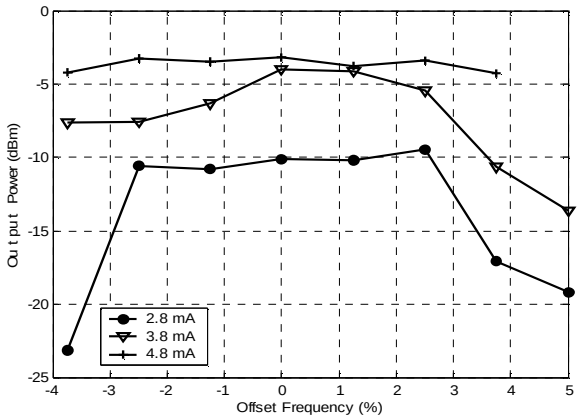

Fig. 5. Output power vs. offset frequency

Fig. 6 says the input-output power transfer function for different values of loop filter pole for the input frequency of 40GHz. It is clear from Fig. 5 that locating the pole of H_F at output frequency (20GHz) results in least required input power for correct division.

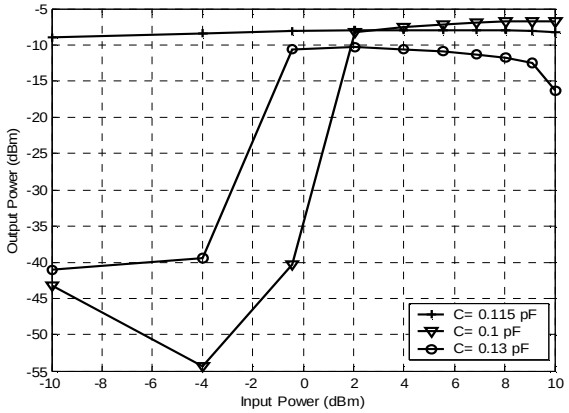

Fig. 6. Output power vs. Input Power

Fig. 7 shows the input and output waveforms for a 40GHz sinusoidal input. Output has a frequency of 20 GHz.

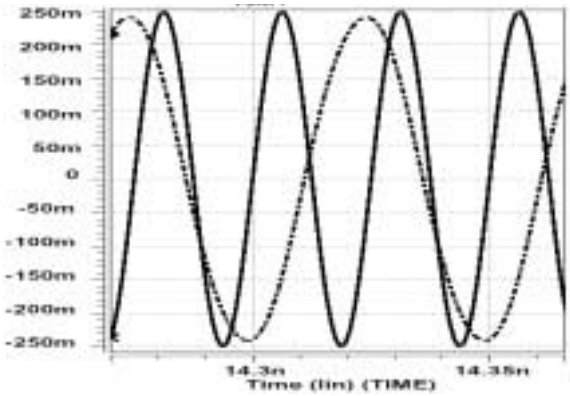

Fig. 7. Input (solid) Output(Dashed) waveforms

Fig. 8 shows the output spectrum for different input power. The arrow depicts the direction of increasing the input. It is evident from Fig. 8 that increasing the input power improves the phase noise .

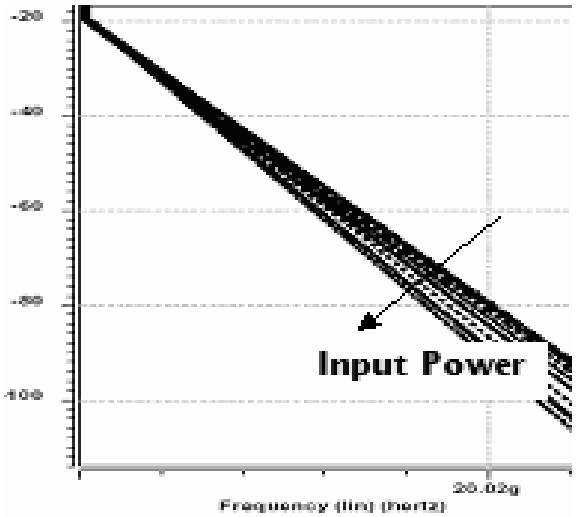

Fig. 8. Output Spectrum for different input powers

4.CONCLUSION

In this paper the design and analysis of distributed regenerative frequency divider (DRFD) based on a novel distributed single-balanced mixer was presented.. Artificial transmission lines were incorporated in distributed single balanced mixer to absorb the parasitic capacitances. The divider shows a division by two for an input frequency of 40GHz while consuming 10-mW from a 1.8-V supply**.**

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