Optimizing the Energy-Delay-Ringing Product in On-Chip CMOS Line Drivers

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Abstract- *This paper presents a detailed empirical study and analytical derivation of voltage wave-form and energy dissipation of global lines driven by CMOS drivers. It is shown that at high clock frequencies where the output voltage at the termination point of the transmission line may not reach its steady state value during the clock period, it is possible to reduce energy dissipation while meeting a DC noise margin by driver sizing. This is in sharp contrast with the steady state analysis, which states that driver size has no impact on the energy dissipation per output change. In addition, we propose a new design metric which is the product of energy, delay and some measure of ringing in lossy transmission lines. In particular, this paper provides closed-form expressions for the energy dissipation, 50% propagation delay and the percentage of maximum undershoot when the circuit exhibits an under-damped behavior. This metric is used during the driver sizing problem formulation for minimum energy-delay-ringing product.*

1. Introduction

New Advances in CMOS technologies has tremendously improved the integration capability and the speed of operation and reduced the amount of energy consumed per signal transition. Technology scaling with 30% reduction in minimum feature size per generation results in: (1) gate delay reduction by 30%, (2) doubling of the number of transistors that fit in the same silicon area (3) energy reduction per transition by 30% to 65% depending on the degree of accompanying supply voltage scaling. These technology-induced improvements, coupled with advances in circuits and microarchitecture design, are expected to continue to support and to sustain the Moore's law until year 2014 [1].

The interconnect structure of a one-billion transistor die will deliver signal and power to each transistor on the chip, provide low-skew and low-jitter clock to latches, flip-flops and dynamic circuits, and also distribute data and control signals throughout the chip [2]. Providing the required global connectivity throughout the whole chip demands long on-chip wires that introduce large loading effects on the drivers. These global wires should deliver high frequency signals (presently at approximately 1.5-2.5GHz) to various circuits. This implies that global wires exhibit transmission line effects. So far, the well-known $0.5CV^2$ model has been used as an interconnect energy model, where C includes the capacitance of the interconnect and the capacitance of the both, the driver and the driven circuits and V is the supply voltage level. This model, however, fails to accurately predict the interconnect energy dissipation in the current range of clock frequencies, where the signal transients do not usually settle to a steady state value due to small clock periods [3].

Consider the circuit shown in Figure 1. If the output voltage reaches the full supply rail level before the signal-level transition, then the energy dissipation per output transition is equal to $0.5CV^2$. From the basic circuit theory, the output of the circuit shown in Figure 1 is either under-damped or over-damped

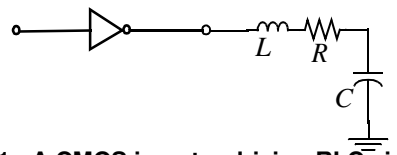

Fig. 1: A CMOS inverter driving RLC circuit

(*cf.* Figure 2). For the under-damped case, if the input starts to change when the output is in the overshoot region, the total energy dissipation per output transition will be larger than $0.5CV^2$. If, on the other hand, the input changes when the output is in the undershoot region, then the energy dissipation is less than $0.5CV^2$. As for the over-damped case, the time-domain behavior is simple due to the monotonic nature of voltage waveforms [4].

In this paper, we provide empirical evidence as well as detailed closed-form analytical expressions for the energy dissipation of a lossy transmission line which is driven by a CMOS inverter and is terminated by a CMOS load. We show that this circuit configuration exhibits behavior similar to the simple example circuit depicted in Figure 1, and therefore, it is possible to reduce energy dissipation, or a given clock frequency by driver sizing. The effect of driver sizing is to change the output behavior (from over-damped to under-damped or vice versa). By careful selection of W/L ratio of the line driver, we may thus reduce the overall energy dissipation of the line and line driver. This is accomplished by forcing the input transition to initiate when the output is in the undershoot region (for the under-damped case), or by forcing the input transition to take place when the output has met the DC noise margin, but not yet reached the steady state (for over-damped case).

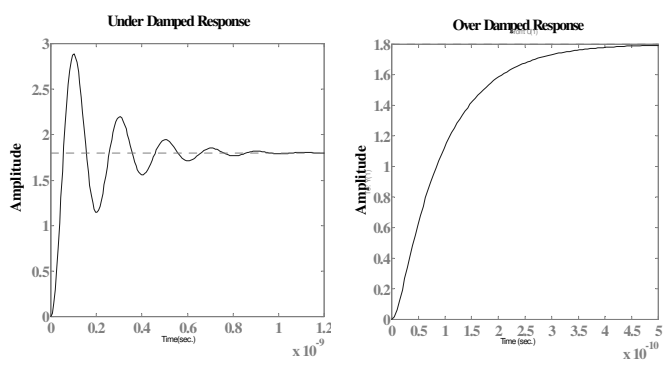

Fig. 2: Under-damped and over-damped response

Of course, there are critical design metrics that need to be taken into consideration during the driver sizing, such as propagation delay and the ringing. We, therefore, present a driver sizing technique that minimizes energy-delay-ringing product. Section 2 gives an overview of a second-order RLC circuit, RLC-π, that accurately models the frequency response of a lossy trans-

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mission line over a wide range of frequencies. Section 3 discusses the voltage and energy characteristics of an interconnect driven by CMOS inverter and the dominant transistor and interconnect parameters that will affect the voltage and energy dissipation. Section 4 gives a new methodologies to find closed-form expressions for the energy dissipation, 50% propagation delay and the percentage of maximum undershoot when the circuit exhibits an under-damped behavior. This metric is used during the driver sizing problem formulation for minimum energy-delay-ringing product in 0.18μm technology [5]. Section 5 shows the results. Finally, conclusions are provided in Section 6.

2. Equivalent Model for Lossy Transmission Line

At the current clock frequencies, the propagation delay of a signal traveling through the chip global wires is comparable to its time of flight. In other words, the line length is comparable to the propagated signal wave-length, λ, which is on the order of 0.6-2.1cm. This implies that transmission line properties at the interconnect must be accounted for [6]. Solutions to Maxwell's equations for the electric and magnetic fields around two parallel conductors (one carrying the signal, the other acting as the current return path) provide the current and voltage wave-forms. The solution is completely determined in terms of the characteristic impedance, Z_o, and the propagation constant,γ, where:

$$Z_0 = \sqrt{\frac{r+sl}{cs}} \quad \text{and} \quad \gamma = \sqrt{(r+sl)\cdot cs} \qquad \textbf{(1)}$$

and r, l, and c are line resistance, inductance, and capacitance per unit length of the interconnect line, respectively. Consider a single lossy transmission line which is driven by a CMOS inverter as shown in Figure 3. The driving point impedance of this transmission line is obtained by using the voltage and current wave-form resulting in the following equations at the input:

$$Z_{in}\Big|_{x=-h} = \frac{V_i e^{\gamma h} + V_r e^{-\gamma h}}{I_i e^{\gamma h} - I_r e^{-\gamma h}} = Z_o\left(\frac{1+\Gamma_L e^{-2\gamma h}}{1-\Gamma_L e^{-2\gamma h}}\right) = Z_o \frac{Z_L + Z_o \tanh(\gamma h)}{Z_o + Z_L \tanh(\gamma h)} \qquad \textbf{(2)}$$

where h is the line length. In CMOS VLSI circuits, the load impedance, Z_L, is normally a capacitive load which can be written as $1/sC_L$. This is because the interconnect normally drives a CMOS circuit element whose input impedance is purely capacitive. According to Eq.(2), the input impedance of a transmission line is a non-linear function of the frequency. Unfortunately, direct substitution of this non-linear expression into the energy equation (which is the integral of the voltage-current product) does not yield a closed-form expression for the energy dissipation of the lossy transmission line. Yet, it is possible to simplify Eq.(1) and obtain an accurate expression for the energy dissipation as described by the following observation.

2.1 First-Order Truncation

If the transitions of the input wave-form are sufficiently spaced apart so as to allow the output wave-form to come very close to its steady state response, then the total energy delivered by the input source can be obtained by using the driving-point impedance of the circuit evaluated at low frequencies. This observation is utilized here to simplify Eq.(2). We approximate tanh(...) at low frequencies by expanding its Taylor expansion around s=0 and truncating higher order terms. The first order Taylor expansion of tanh(γh) is γh. This leads to the following approximate rational function [4]:

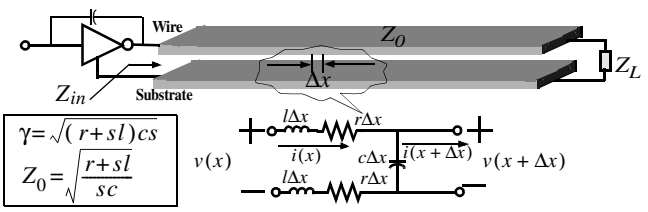


Fig. 3: A lossy transmission line driven by a CMOS inverter along with the circuit representation for an infinite small segment *ΔX* along the line

$$Z_{in}\Big|_{x=-h} = \frac{1}{C_L s}\left[\frac{1+\left(\gamma^2 h^2 \frac{C_L}{C_{int,tot}}\right)}{1+\frac{C_{int,tot}}{C_L}}\right] \qquad \textbf{(3)}$$

where $C_{int,tot}$ is the total interconnect capacitance including the area of fringing capacitance as well as the coupling capacitance to neighboring lines. Using Eq. (3), a series *RLC* circuit is synthesized as shown in Figure 4 where L_{eq} and R_{eq} are defined as follows:

$$R_{eq} = \frac{C_L}{C_L + C_{int,tot}} R_{int}\ , \qquad L_{eq} = \frac{C_L}{C_L + C_{int,tot}} L_{int,tot} \qquad \textbf{(4)}$$

$$C_{eq} = C_{int,tot} + C_L$$

where R_{int} is the line resistance and $L_{int,tot}$ is the total inductance of the lossy line. $L_{int,tot}$ is calculated by summing self inductance of the line and all mutual inductances between that line and other lines considering the direction of the current flow through the lines.

2.2 Second-Order Truncation

The second-order truncation of the Taylor series expansion of tanh(γh) is [4]:

$$\tanh(\gamma h) = \frac{\sinh(\gamma h)}{\cosh(\gamma h)} \rightarrow \frac{2\gamma h}{2+\gamma^2 h^2}, \text{ for small values of } |s|.$$

This leads to the following relationship [4]:

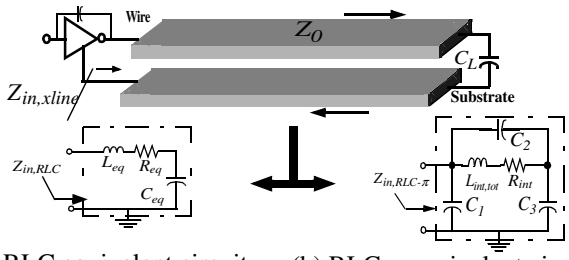
$$Z_{in}\Big|_{x=-h} = \frac{1}{C_L s}\left[\frac{2+\gamma^2 h^2 + \left(2\gamma^2 h^2 \frac{C_L}{C_{int,tot}}\right)}{2+\gamma^2 h^2 + \left(2\frac{C_{int,tot}}{C_L}\right)}\right] \qquad \textbf{(5)}$$

It would be instructive and useful to drive a stable circuit realization whose impedance is expressed by Eq.(5). It is easily proven that for a lossy transmission line whose driving-point impedance at lower frequencies is expressed by Eq.(5), a new stable *RLC*-π equivalent circuit realization with an identical input impedance can be synthesized. The circuit structure is depicted in Figure 4.b. C_1^E, C_2^E, and C_3^E are related to the actual energy *RLC*-π model capacitances of the line and the load through the following relationships [4]:

$$C_3^E = \sqrt{\frac{(C_{int,tot} + C_L)^2 + C_L^2}{2}}\ , \quad C_2^E = \frac{C_{int,tot}}{2} + C_L - C_3^E \qquad \textbf{(6)}$$

$$C_1^E = C_{int,tot} + C_L - C_3^E$$

Figure 5 shows the magnitude response of the driving-point admittance of a lossy transmission line which is electromagnetically coupled to a similar line [4]. The line electrical parameters



(a) RLC equivalent circuit (b) RLC-π equivalent circuit

Fig. 4: A lossy transmission line and its equivalent circuit representations

are also indicated in Figure 5. First, the circuit is simulated using star-HSPICE. Eq.(2) is then utilized and the magnitude response of the admittance function is calculated. As indicated in Figure 5, the results obtained by HSPICE and by Eq.(2) are exactly the same and are indistinguishable from each other.

In the next step, the magnitude response of the driving-point admittance of the equivalent *RLC-π* circuit is calculated. According to Figure 5, this circuit accurately represents the driving-point admittance of a lossy coupled transmission line in lower frequencies up to 32GHz.

Therefore, the energy calculations using the RLC-π circuit yield expressions that are exactly equal to those of the actual coupled lossy line. Finally the magnitude response of the driving-point admittance of the equivalent RLC circuit is calculated and compared with those of RLC-π equivalent circuit and the lossy coupled line, as is also shown in Figure 5. The RLC-π circuit models the lossy line more accurately than the RLC circuit in a broader range of frequencies.

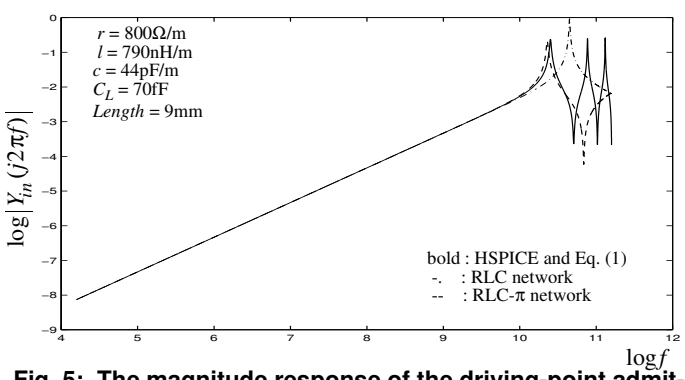


Fig. 5: The magnitude response of the driving-point admittance of an electromagnetically coupled lossy transmission line obtained using HSPICE simulation, using the direct simulation of Eq.(1), and by replacing the line with its equivalent RLC-π circuit, and with its equivalent RLC circuit

Using the same second-order truncations for voltage transfer function, which can be written as:

$$H_v\Big|_{x=-h} = \frac{Z_L}{Z_o\cosh(\gamma h) + Z_L\sinh(\gamma h)} \qquad \textbf{(7)}$$

The equivalent delay RLC-π model values would be:

$$C_1^D = \frac{C_{int,tot}}{2}, \quad C_2^D = 0, \quad C_3^D = \frac{C_{int,tot}}{2} + C_L,$$

$$L_{eq}^D = L_{int,tot}, \quad R_{eq}^D = R_{int,tot}$$

Section 3 provides a discussion about how the energy, delay and ringing of a circuit changes with driver sizing. Section 4 provides comprehensive analysis of delay and energy dissipation of the lossy transmission lines driven by CMOS inverters.

3. Output Voltage and Energy Dissipation as a Function of Driver

Consider a transmission line which is driven by a CMOS inverter and is terminated by a CMOS load. The output voltage wave-form at the load varies significantly as a function of driver *W/L* ratio. In practice, the output behavior may change from an over-damped response towards an under-damped response. In other words, although the steady state output voltage values are the same, the transient wave-forms are drastically different depending on the electrical parameters of the line and line driver. Note that energy dissipation varies as a function of the clock cycle time. If the output wave-form has not reached its steady state at the clock edges, the amount of energy dissipation in the clock cycle may be lower (if in the undershoot region) or higher (if in the overshoot region, when exhibiting under-damped behavior) compared to the steady state value of $0.5CV^2$.

V_{out} variations for four different driver *W/L* ratios are shown in Figure 6. Figure 7 shows the energy dissipation variation per clock period for different driver *W/L* ratios.

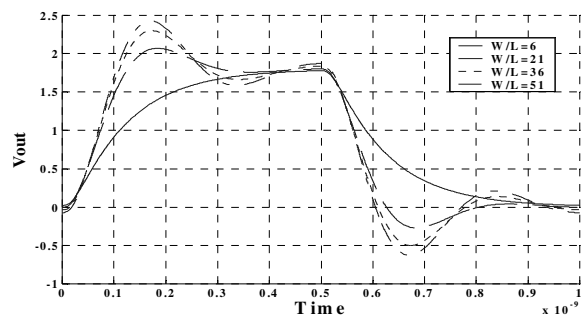


Fig. 6: V_{out} as a function of four different driver *W/L* ratios

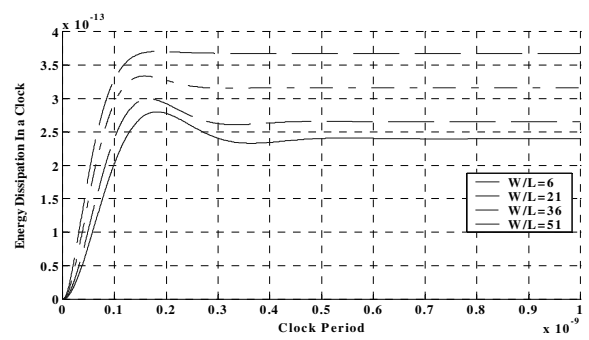


Fig. 7: Energy dissipation in a clock cycle as a function of the clock period for four different driver *W/L* ratios

Therefore, by changing the *W/L* ratio of the driver we can change the characteristics of the output voltage and thereby, the amount of energy dissipation per clock period. There are three crucial design metrics to consider:

1. Energy dissipation in a clock period
2. 50% propagation delay of V_{out}
3. Degree of undershoot in an under-damped response which should be less than the noise margin (in a low-to-high transition, the noise margin is approximately $|V_{Tp}|$)

From Figure 6, we observe that the over-damped response does not exhibit ringing, but exhibits a large delay. The under-damped response has lower delay, but may cause DC noise margin violations. Nonetheless, the 50% propagation delay is not a good metric for an under-damped system due to the existence of damped oscillations. To take the effect of the circuit delay into account, we propose a new metric. For the over-damped response since all the wave-forms are monotonically rising or falling wave-forms, the best performance metric is the *energy-50% delay* product. However, for the under-damped response the delay must incorporate the settling time of the oscillations as well as the percentage of maximum undershoot for noise-margin violations. To come up with a unique metric for both the under-damped and over-damped responses, we use the *energy-50% delay-(1+undershoot%)* product. Considering "*1+undershoot%*" as ringing factor, we call the cost function, "*EDR* product". Figure 8 shows the *EDR* product per clock cycle of an inverter driving a lossy transmission line with a pure capacitive load termination. The small incremental positive slope of the *EDR* product metric with respect to the *W/L* is due to the direct relationship between the energy and the diffusion capacitance of the device.

As shown in Figure 8, *EDR* product changes for different driver *W/L* ratios and also it is dependent to clock period according to Figure 7. Figure 8 shows that for a determined interconnect width, always there is an optimum driver W/L which minimizes the *EDR* product. The key to minimize *EDR* product is to find output wave-form and energy dissipation which will be discussed in section 4.

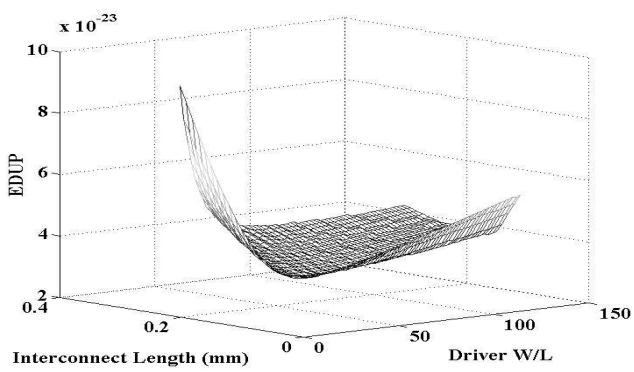


Fig. 8: *EDR* product variation per clock period for different interconnect widths and driver *W/L* ratios

4. Driver Sizing for Optimum *EDR* Product

4.1 Analytical Derivation of Output Voltage and Energy Dissipation

Authors of [4] attempted to find the optimum driver size for minimizing the *EDR* product. However, because they could not find a unified closed-form expression for energy, delay and ringing, they were not able to obtain an analytical solution for the optimum drive size. In contrast, in this paper, we provide a closed-form driver sizing solution that minimizes the *EDR* product.

Consider the circuit in Figure 3, which is composed of an inverter driving a lossy transmission line. The load is another CMOS gate that is connected to the output port of the lossy transmission line. The electromagnetic coupling effects are treated the same way as discussed in Section 2. Due to the changes in the operation regions of the NMOS and PMOS transistors of the line driver during the low-to-high and high-to-low transitions of the driver's output, we must distinguish between low-to-high and high-to-low transitions at the output. The PMOS transistor is conducting and provides a low-impedance conduction path from the supply to the load. During the high to low transition at the output, the NMOS transistor is in the "ON" position and no additional energy is transferred out of the power supply.

We calculate the energy transferred out of the power supply during a low-to-high transition. This energy is the total energy dissipated per clock period of a CMOS gate that drives another CMOS circuit through a lossy coupled transmission line. The energy delivered by the power supply through the gate in a low-to-high transition of the output is specified as follows:

$$E_{total} = \int_{t=0}^{\frac{T}{2}} V_{DD}\, I_{in}(t)dt \qquad \textbf{(8)}$$

where $I_{in}(t)$ is the current flowing from the power supply to the load and through the PMOS transistor during the low-to-high transition of the output. The current is obtained using the driving-point admittance of the circuit:

$$I_{in}(s) = \frac{V_{DD}}{s} Y_{in}(s) \qquad \textbf{(9)}$$

where $Y_{in}(s)$ is the driving-point admittance seen from the power supply to the source connection of the PMOS transistor of the driver. Figure 9 shows the equivalent simplified model of the circuit shown in Figure 3.

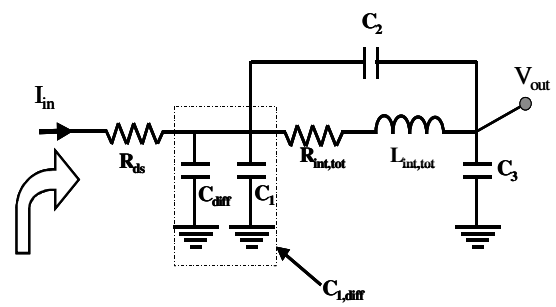


Fig. 9: Equivalent circuit for the transmission line driven by a CMOS inverter

Considering $C_{1,diff}=C_1+C_{diff}$, if we write the transfer function of the circuit, we have:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0} \qquad \textbf{(10)}$$

where:

$$a_2 = L_{int}C_2^E \qquad a_1 = R_{int}C_2^E \qquad a_0 = 1$$

$$b_3 = R_{ds}L_{int}(C_{1,diff}^E C_2^E + C_{1,diff}^E C_3^E + C_2^E C_3^E)$$

$$b_2 = L_{int}(C_2^E + C_3^E) + R_{ds}R_{int}(C_{1,diff}^E C_2^E + C_{1,diff}^E C_3^E + C_2^E C_3^E)$$

$$b_1 = R_{ds}(C_{1,diff}^E + C_3^E) + R_{int}(C_2^E + C_3^E) \qquad b_0 = 1$$

From Eq.(10) it is seen that the system is represented using a third-order transfer function equation. It is hard to derive a closed-form expression for energy and delay of a such a system. On the other hand, for different interconnect lengths and driver *W/L*s, the output voltage of the circuit behaves like a second-order circuit over the frequency range of interest. Several experiments using practical geometrical values of an interconnect and

line driver in CMOS VLSI circuits prove that the magnitude of b_3s^3 appeared in the transfer function is small compared to other coefficients during frequencies of interest. The results are shown later. Then, we can neglect the effect of b_3 and use the approximation as shown below:

$$\frac{V_{out}(s)}{V_{in}(s)} \cong \frac{a_2s^2 + a_1s + a_0}{b_2s^2 + b_1s + b_0} \quad \textbf{(11)}$$

Consequently, we can approximate the third-order circuit with a second order circuit and find closed-form expressions for the output wave-form and the energy of the system. This approximation follows the circuit behavior very well in deep sub-micron technologies. As an example, Figure 10 shows the approximated output wave-forms for two different lengths and driver *W/Ls*, when we apply step function to the input of the driver. For different interconnect lengths and driver *W/L*s, the average error between actual output and approximated output wave-forms is shown in Figure 11. The errors between real output voltage (V_{out}) and approximated output voltage (V^*_{out}) are calculated as below:

$$error = \frac{\int_0^T (V_{out} - V^*_{out})^2 dt}{\int_0^T V^2_{out}\, dt} \quad \textbf{(12)}$$

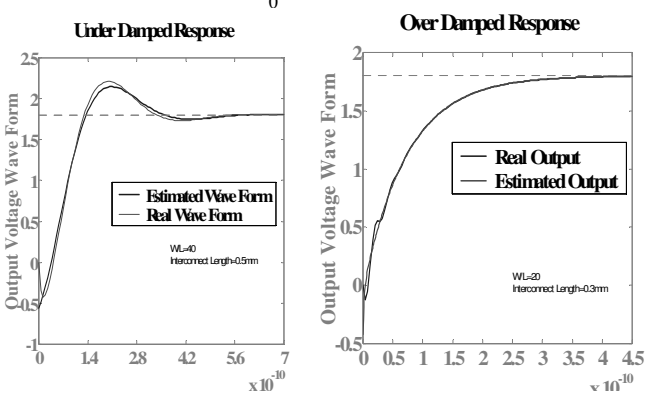


Fig. 10: The comparison between real output voltage and approximated one for both under-damped and over-damped cases

The average error for all the data from 2050 simulation results is 0.93% in 3 different frequency ranges, 1GHz, 1.66Ghz, and 2GHz. The maximum error was 3.4%. Therefore, instead of solving the problem as a third order transfer function, we can indeed use the equivalent second-order formulation and find the output wave-form. Similarly for I_{in}, we have:

$$\frac{I_{in}(s)}{V_{in}(s)} = \frac{d_3s^3 + d_2s^2 + d_1s}{b_3s^3 + b_2s^2 + b_1s + b_0} \quad \textbf{(13)}$$

$$= 1 - \frac{L_{int}(C_2^E + C_3^E)s^2 + R_{int}(C_2^E + C_3^E)s + 1}{L_{int}C_2^E s^2 + R_{int}C_2^E s + 1} \times \frac{V_{out}(s)}{V_{in}(s))}$$

where:

$$d_3 = L_{int}(C^E_{1,diff}C^E_2 + C^E_{1,diff}C^E_3 + C^E_2C^E_3)$$
$$d_2 = R_{int}(C^E_{1,diff}C^E_2 + C^E_{1,diff}C^E_3 + C^E_2C^E_3)$$
$$d_1 = C^E_{1,diff} + C^E_3$$

If we substitute the approximated transfer function in Eq.(11) in Eq.(13), we obtain:

$$\frac{I_{in}(s)}{V_{in}(s)} = \frac{d_2s^2 + d_1s}{b_2s^2 + b_1s + b_0} \quad \textbf{(14)}$$

At this point, we have found equivalent second order equations for both I_{in} and V_{out}.Then based on equations (11) and (14), the closed-form expressions for I_{in} and V_{out} are as follows:

A. Over-damped Response

$$V_{out}(t) = V_{DD}(1 + e^{-\alpha t}(k_1\sinh(\omega_d t) + k_2\cos h(\omega_d t))) \quad \textbf{(15)}$$

$$Energy = (C^E_{1,diff} + C^E_3)V^2_{DD} - V^2_{DD}\cdot e^{-\alpha t}(k_3\sinh(\omega_d t) + k_4\cosh(\omega_d t))$$

where:

$$k_1 = \frac{a_2}{\omega_d}\left(\omega_n^2\left(\frac{a_1}{a_2} - \alpha\right) - \frac{\alpha}{a_2}\right) \quad k_2 = a_2\left(\omega_n^2 - \frac{1}{a_2}\right) \quad k_3 = \frac{d_2}{\omega_d}\left(\frac{d_1\alpha}{d_2} - \omega_n^2\right)$$

$$k_4 = -d_1 \qquad \omega_n = \sqrt{\frac{b_0}{b_2}} \qquad \alpha = \frac{b_1}{2b_2} \qquad \omega_d = \sqrt{\alpha^2 - \omega_n^2}$$

a_i, b_i and d_i are coefficients of the transfer functions.

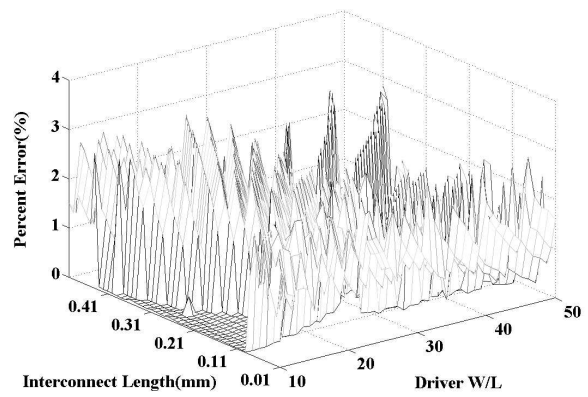


Fig. 11: Average error between real output wave-form and approximated wave-form

B. Under-damped Response

$$V_{out}(t) = V_{DD}(1 + e^{-\alpha t}(k_1\sin(\omega^o_d t) + k_2\cos(\omega^o_d t))) \quad \textbf{(16)}$$

$$Energy = (C^E_{1,diff} + C^E_3)V^2_{DD} - V^2_{DD}\cdot e^{-\alpha t}(k_3\sin(\omega_d t) + k_4\cos(\omega_d t))$$

where the expressions k_1, k_2, k_3, k_4, $\omega n, \alpha$ are the same as described above and

$$\omega^o_d = \sqrt{\omega_n^2 - \alpha^2}$$

4.2 Analytical Derivation of Delay and Ringing

In the case of under-damped, we have ringing. To find the optimum point in *EDR* product, we need to find the 50% delay and ringing, too. Per reference [7], 50% delay can be calculated by computing the first four moments of the voltage transfer function, accurately. The first four moments of the voltage transfer function are:

$$m_0 = 1, \qquad m_1 = -\left(R_{int}C^D_3 + R_{ds}\left(C^D_{1,diff} + C^D_3\right)\right) \quad \textbf{(17)}$$

$$m_2 = m_1^{\,2} - C_3^D\left(L_{int} + R_{ds}R_{int}C_{1,\,diff}^D\right)$$

$$m_3 = m_1 m_2 + C_3^D\left[\left(L_{int} + R_{ds}R_{int}C_{1,\,diff}^D\right)C_3^D(R_{ds} + R_{int}) + R_{int}\left(R_{ds}C_{1,\,diff}^D\right)^2\right]$$

Using these moments iin reference [7] delay equations, we can find an accurate value for 50% propagation delay.

There is no ringing for over-damped case, while the ringing of the under-damped response, at the point the output waveform reaches its first minimum, is given by:

$$Ringing = 1 + \frac{V_{out}\left(\frac{4\pi}{\omega_d}\right)}{V_{DD}} \qquad \textbf{(18)}$$

4.3 Driver Sizing for Optimum *EDR* Product

Using equations (15)-(18), we can calculate the *EDR* product for a circuit. Consider $R_D=k_R/W_D$ and $C_{diff}=k_C W_D$, where k_R and k_C are constants that are dependent on the technology, and W_D is the driver size. The optimum driver sizing solution is solved by solving the following non-linear equation:

$$\frac{d}{d(W_D)}(EDRP) = 0 \qquad \textbf{(19)}$$

5. Experimental Results

Comparison between our analytical predictions for delay and energy with HSPICE simulations are reported in Figures 12 and 13, respectively. From these experiments, it can be seen that for different interconnect widths and driver sizes, our delay equation exhibits very high accuracy (i.e., only 1.7% average error) and that the energy equation shows a mere 4.3% average error.

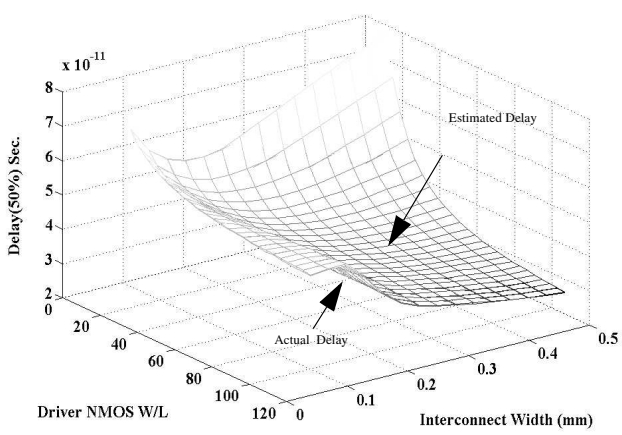


Fig. 12: The comparison between 50% propagation delay and the obtained formulation for both under-damped and over-damped cases

6. Conclusion

This paper presented accurate expressions for the interconnect energy dissipation and propagation delay in high performance ULSI circuits. We showed that at high clock frequencies, where the output voltage at the termination point of a transmission line, does not reach its steady state value during the clock period, it is possible to reduce energy dissipation while meeting a DC noise margin by driver sizing. It was shown that this phenomenon is mostly due to the voltage behavior of the transmission line at its termination point which may correspond to either under-damped or over-damped behavior. More precisely, if the clock period is chosen such that the output voltage for the under-damped case is in its overshoot region, then energy dissipation per transition in the clock cycle will be higher than $0.5CV^2$. On the other hand, if the output voltage is in the undershoot region when the clock changes, the energy dissipation per transition in the clock cycle will be lower than $0.5CV^2$. Of course for the over-damped case, energy is always less than or equal to $0.5CV^2$. In addition, we propose a new design metric which is the product of energy, delay, and ringing in lossy transmission lines. This metric is used during the driver sizing problem formulation.

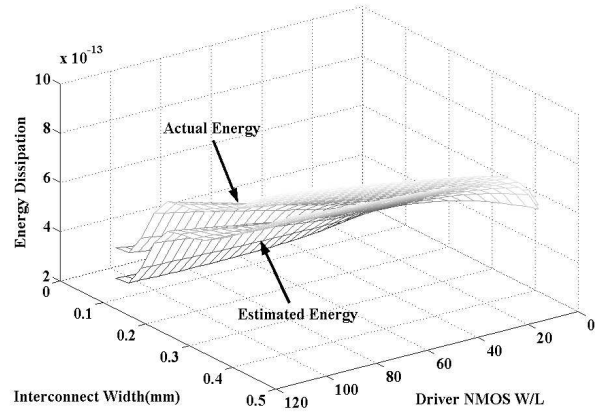


Fig. 13: The comparison between real energy and approximated one for both under-damped and over-damped cases

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