Analysis of DLL Jitter Due to Substrate Noise

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Abstract - *Substrate noise is the major source of performance limitation in mixed-signal integrated circuits. This paper studies substrate noise effects on the performance of delay-locked loops (DLLs). Due to their robust noise performance, the delay-locked-loops are widely used as clock generators of microprocessors. Although exploiting advanced circuit techniques reduces the timing jitter induced by the substrate noise to a large extent, the hostile noisy digital section in a mixed-signal VLSI circuit can still cause a large substrate noise and hence a non-negligible timing jitter in DLL clock generators. In this paper a new stochastic model for the substrate noise is proposed. This model is then utilized to derive the phase noise of the voltage-controlled delay line (VCDL) inside the loop. The DLL timing jitter is predicted in response to the VCDL phase noise. A comparison between the results obtained by our mathematical model and those obtained using HSPICE verifies our proposed model.*

1. Introduction

The continued scaling of CMOS technology together with progress in the design of high-frequency analog and mixed-signal CMOS circuits has enabled the designers to implement many functions onto a single chip. One of the greatest challenges in the design of such systems is a need to put broadband analog circuits on the same die that the large complex digital signal processing components are placed. Due to the high-level of interactions between the noisy digital blocks with the noise sensitive analog parts through various propagation mechanisms it is highly possible that the large-signal switching transients of the digital circuits corrupt the performance of the analog sub-blocks. Crosstalk from digital circuits on analog components is mostly via substrates and thus named the substrate noise. Such noise degrades analog signal integrity in mixed-signal integrated circuit design [1] [2]. Substrates comprised of a lightly doped epitaxial layer grown on a heavily doped substrate will exhibit a good performance in minimizing the latch-up phenomenon, and as a result these types of substrates are widely used in system-on-chip (SOC) [3]. However, there is an increasing trend to use silicon-on-insulator technology to due its superior power dissipation performance. In general, the substrate noise propagation through the silicon bulk is a complicated phenomenon and strongly depends on the substrate doping profiles. However, since the resistivity of the heavily doped p+ substrate in a low epitaxial layer is quite low, such substrates are generally modeled as a single node [3]. Thus, the substrate propagation is approximately uniform throughout the heavily doped substrate. The building blocks that are exposed to the substrate noise are clearly the ones that provide the communication interface between the digital part and the analog part, namely analog-to-digital (A/D) and digital-to-analog (D/A) converters, as well as the clock generator of the digital synchronous circuit.

Delay-locked loops (DLLs) are widely utilized as on-chip clock frequency generators to synthesize a low skew and higher internal frequency clock from an external lower frequency signal and also as clock and data recovery circuits (CDR) in broadband communications systems. The random temporal variation of the phase, or jitter, is a critical performance parameter in the design of DLL circuits. A delay-locked loop circuitry exhibits a better noise performance than a phase-locked loop (PLL), and therefore it is widely used as a clock generator in a mixed-signal integrated circuit where the noisy digital circuits will severely affect the analog portion through the noise being injected through the silicon substrate.

In this paper we focus on the charge-pump DLL due to its widespread use in today's frequency synthesizers and clock generators for microprocessors. The contribution of the present paper is as follows:

- Predicting the timing jitter of a DLL in terms of the phase noise of the voltage-controlled delay line (VCDL) resulting from the substrate noise. This is accomplished by using a stochastic model for the substrate noise.

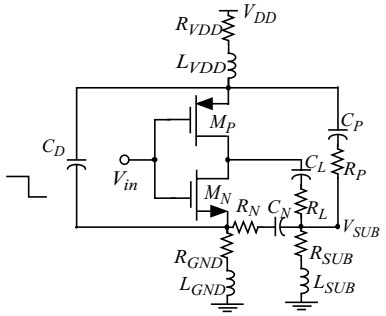
The outline of the paper is as follows. Section 2 presents a new mathematical model for the substrate noise. Section 3 relates the VCDL phase noise to the statistical properties of the substrate noise. The effect of the VCDL noise on the DLL output phase is accounted for. Finally, section 4 presents the conclusions of our paper.

2. Substrate Noise Characterization

In this section, first, we briefly explain a simple model to characterize the substrate noise in mixed-signal integrated circuits.

In a CMOS mixed-signal integrated circuit the substrate is normally composed of a lightly doped epitaxial layer grown on a heavily doped substrate in order to minimize the transistor latch-up [3]. On the other hand, in the silicon-on-insulator (SOI) technology a thin layer of substrate is grown on top of an insulator such as silicon oxide or glass to reduce the parasitic junction capacitances of the MOS device and thus reduce the power dissipation. In both technologies the injected lateral current from the source of a digital circuit (e.g., a CMOS inverter) flows in the heavily doped substrate because of its low resistivity compared to the inter-layer silicon or epitaxial layer [3]. The bulk can thus be modeled as a single electrical node.

Most CMOS logic elements can be reduced or decomposed into CMOS inverters. Therefore to study the substrate noise as a function of the digital circuit characteristics, the substrate noise caused by a single transition in a CMOS inverter is first examined. Fig. 1 shows the circuit utilized to model the substrate noise injection with p+ substrate represented by a single electrical node.



0.18μm standard CMOS
LGND = *LVDD* = 4nH
RGND = *RVDD* = 3
LSUB = 3nH
RSUB = 1
CD = 2pF
CP = 300fF
RP = 3
CL = 400fF
RL = 2
CN = 200fF
RN = 2

Fig. 1. The circuit model for the substrate noise injection

In Fig. 1 R_{GND} , L_{GND} and R_{VDD} , L_{VDD} are power/ground inductance and resistance modeling the chip-package. R_{SUB}, L_{SUB} represents the substrate bias impedance. R_N , C_N are the equivalent capacitance and resistance from the chip ground to the heavily doped substrate including the wiring capacitance and junction capacitance of NMOS. R_P , C_P are the equivalent resistance and capacitance from the chip power supply to the heavily doped substrate including the nwell junction capacitance and the nwell physical resistance. R_L , C_L are the equivalent load resistance and capacitance including the gate capacitance of the following fan-out stages. C_D is the on-chip decoupling capacitor. Since the substrate is tightly coupled to the return path by distributed surface substrate contacts, the voltage bounce arising from this process, especially on the ground path, appears as the substrate noise. Fig. 2 shows the result of the HSPICE simulation performed on the circuit shown in Fig. 1.

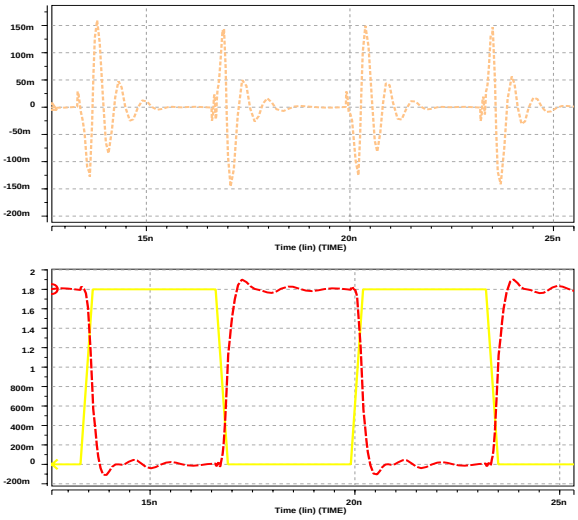
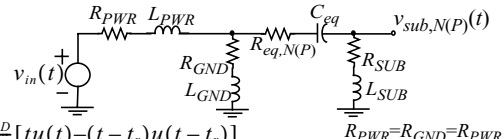


Fig. 2. (upper) The substrate noise variation in a single inverter designed in 0.25µm standard CMOS process

Our goal is to provide a simple closed form expression for the substrate noise that later on will be utilized to investigate the DLL jitter. To achieve this goal it is assumed that each transistor operates either in the triode region (when it turns on) or in the cutoff region (when it turns off) during the entire low-to-high or high-to-low signal transition. In practice, each transistor experiences operating-region transitions throughout the low-to-high or high-to-low input transition [4][5]. Under this assumption, equivalent circuits for each signal transition are constructed. Fig. 3 shows such a circuit and its corresponding transfer function.



$$v_{in}(t) = \frac{V_{DD}}{t_r}[tu(t)-(t-t_r)u(t-t_r)]$$

$R_{PWR}=R_{GND}=R_{PWR,G}$
$L_{PWR}=L_{GND}=L_{PWR,G}$

$$C_{eq}=C_L+C_P+C_N\ ;\ R_{eq,N}=(R_L+R_{NMOS})\|R_N\|R_P\ ;\ R_{eq,P}=(R_L+R_{PMOS})\|R_N\|R_P$$

$$V_{sub,N(P)}(s) = \frac{V_{DIV}(1-e^{-st_r})}{t_r\, s}\,\frac{s+1/\tau_z}{s^2+2\zeta_{N(P)}\omega_0 s+\omega_0^2}$$

$$V_{DIV} = V_{DD}\frac{L_{SUB}}{L_{PWR,G}+2L_{SUB}}\ ;\ \omega_0 = \frac{1}{\sqrt{(L_{SUB}+L_{PWR,G}/2)C_{eq}}}\ ;\ \tau_z = \frac{L_{SUB}}{R_{SUB}}$$

$$\zeta_{N(P)} = \frac{R_{eq,N(P)}+R_{SUB}+R_{PWR,G}/2}{2}\sqrt{\frac{L_{SUB}+L_{PWR,G}/2}{C_{eq}}}$$

Fig. 3. A simplified circuit model for the substrate noise

From this representative circuit model it is observed that the substrate noise is mainly dominated by the fluctuations on the power/ground rails. This observation is also experimentally verified [1]. In fact, the simulations with 1nH and larger inductors shows a much larger substrate noise due to the noise coupling from the supply and ground rails.

In practice, the substrate noise is caused by random switching pattern of digital switching circuits on a chip. The switching activity of a large digital circuit is a function of the nature and the statistics of the input signals. as a consequence, the substrate noise, $v_{sub}(t)$ is a stochastic process.

To characterize the statistics of substrate coupling due to the circuit switching, we first note that if the analog and digital circuits are separated by at least four times the thickness of the epitaxial layer, the resistance between the substrate contacts will be independent of their separation [3]. Therefore the spacing between the switching blocks causes a random phase shift on the noise fluctuations only. The peak amplitudes of damped oscillations for each noise waveform $v_{sub,N}(t)$ and $v_{sub,P}(t)$, are a function of switching activities of digital circuits and are thus represented by discrete-time random processes.

The above observations are utilized to derive a mathematically robust and efficient stochastic model for the substrate noise:

$$v_{sub}(t)=\sum_{n=-\infty}^{[t/T]}A_{sub,N}[n]\,v_{sub,N}(t-nT-\lambda_n)+\sum_{n=-\infty}^{[t/T]}A_{sub,P}[n]\,v_{sub,P}\left(t-nT-\frac{T}{2}-\gamma_n\right) \quad (1)$$

The substrate noise is comprised of two additive terms, one is due to the low-to-high signal transition, and the second one is due to the high-to-low signal transition. $A_{sub,N(P)}$ is a discrete-time random process that accounts for the number of adjacent switching circuits switching simultaneously. λ_n and γ_n are a set of normally distributed independent random variables in the interval $[0, T]$. their presence in the noise expression is because the digital circuits across the chip switch in a random fashion. The random switching of the digital blocks manifest itself as a random propagation delay to a sensitive analog point such as a data converter. The analysis can easily be extended to a more general scenario in which there are multiple clock frequencies across the digital circuit. Theorem 1 proves useful in determining the spectral contents of $v_{sub}(t)$.

Theorem 1. Consider the following wide-sense cyclo-stationary stochastic process:

$$x(t)=\sum_{n=-\infty}^{\infty}A[n]\,v(t-nT)$$

where $A[n]$ is a discrete-time random-process. The shifted process $z(t)$:

$$z(t)=\sum_{n=-\infty}^{\infty}A[n]\,v(t-nT-\lambda_n)$$

is a wide-sense stationary process, whose power spectral density is:

$$S_z(\omega)=\frac{1}{T}S_A(e^{j\omega})|V(\omega)|^2 \quad (2\text{-a})$$

Proof: This theorem is an extension of Theorem 2 in pp. 374 of the reference [6]. ❐

Using Theorem 1 and Eq. (2-a) the power spectral density of the substrate noise is obtained as follows:

$$S_{sub}(\omega)=\frac{1}{T}[\,S_{A_{sub,N}}(e^{j\omega})|V_{sub,N}(\omega)|^2+\,S_{A_{sub,P}}(e^{j\omega})|V_{sub,P}(\omega)|^2] \quad (2\text{-b})$$

3. DLL JITTER

To experimentally emulate the switchings of digital circuits, 10 tapered inverters driving large 2pF capacitors are placed around the DLL circuit. In this section we briefly study the timing jitter induced by substrate noise in closed-loop delay-locked loops. Papers [7], [8], [9] discuss the PLL timing jitter in more depth and details. The jitter and phase noise in a free-running is not discussed. The reader is referred to [9] and [10] for a detailed look at the phase noise in oscillators.

The main focus of the analysis is on charge-pump DLLs, although the analysis is easily extended to any type of delay-locked loop. Furthermore, the DLL circuit has a fully differential signal path in order to reduce the noise sensitivity of the DLL closed-loop system to the substrate and power-supply noise sources. Fig. 3 shows a simplified system block diagram of a charge-pump DLL circuit.

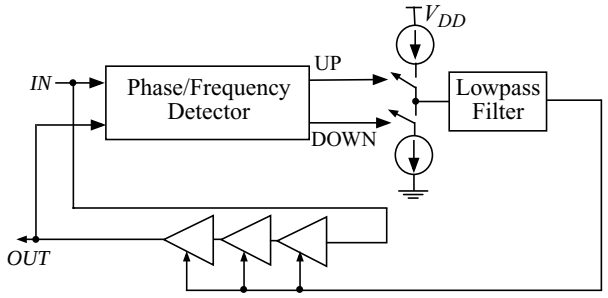


Fig. 3. A system block diagram of the charge-pump DLL

In a differential architecture the voltage-controlled delay line (VCDL) circuit is the most noise sensitive circuit among other sub-blocks. The reason is that the VCDL normally consists of an open-loop differential delay line where corrupted zero-crossings of the oscillations due to the substrate or supply noise propagate though the delay stages and appear at the end of the delay line. If the phase jitter lies in the lock-range of the DLL, the DLL ultimately responds to the phase jitter such that the jitter will disappear at the end of the delay line. Furthermore, the fast jitter components generated by the VCDL is not suppressed by the DLL. On the other hand, the jitter coming from the input terminal does not have much of an effect because firstly, in a DLL-based clock generator the input is coming from a very low jitter source and secondly, the DLL filters out the in-band components of the input jitter.

A differential VCDL consists of N differential stages. A differential architecture will have better power-supply rejection ratio (PSRR) and a superior noise performance compared to a single-ended ring architecture. Each delay stage produces a pair of large-signal differential waveforms that drive a similar delay stage within the VCDL path. Each MOS transistor of the differential source-coupled pair will thus experience a large-signal gate voltage and therefore it will exhibit a multiple transition of the region of operation. Moreover, the I_D-V_{GS} relationship of a MOS transistor is non-linear for both triode and saturation regions. All these phenomena cause the VCDL delay to be a nonlinear function of the supply and input control voltages. This nonlinear relationship is also dependent on the circuit topology of each delay stage. In most of the current proposed differential delay architectures the VCDL gain is controlled by the current tail due to achieving a wider tuning range and a roughly linear frequency-voltage relationship. A simplified circuit topology commonly used in each delay stage is shown Fig. 4. The resistors R_D can be implemented using PMOS loads operating as a voltage controlled resistors to make the voltage swings independent of the supply variations.

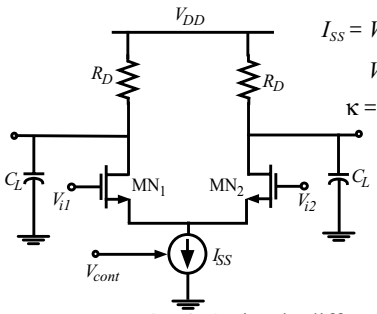
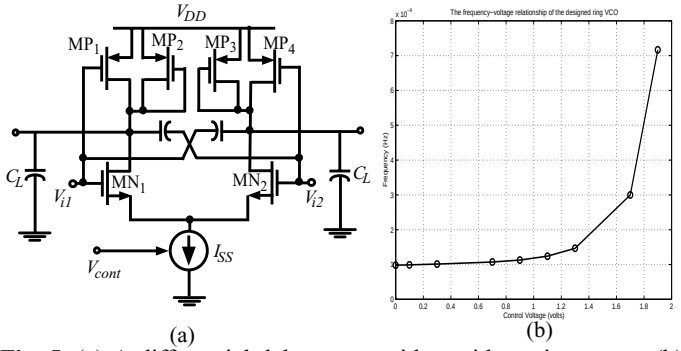


Fig. 4. A simple differential delay stage

Using the BSIM3V3 MOS model, the value of the current I_{SS} is:

$$I_{SS} = W\upsilon_{sat}C_{ox}(V_{cont} + v_{cont,sub} - v_{tr,sub} - V_{TH} - V_{DS,sat}) \quad (6)$$

According to Eq. (6) the substrate noise affects the current produced by the current tail through the control path, and through the direct substrate coupling to the NMOS and PMOS transistors. The former is reduced using a differential control input with the latter being almost intact. Since the velocity-saturated drain-source voltage, $V_{DS,sat}$, is also a nonlinear function of the gate-source voltage, the tail current becomes a nonlinear function of the substrate noise which introduces harmonic distortion at the DLL output. To verify this observation a five-stage fully differential VCDL is designed where each delay stage is implemented using the circuit given in Fig. 5. The feedback capacitors in the circuit shown in Fig. 5 are provided to increase the tuning range of the delay stage, lower the free-running frequency, and more importantly to neutralize the input-output coupling caused by C_{GD} capacitance.



(a) (b)

Fig. 5. (a) A differential delay stage with a wide tuning range. (b) the delay-voltage characteristics of the five-stage differential VCDL

The VCDL oscillations in the presence of the substrate noise will experience distortions. as also shown in Fig. 6.b. The substrate noise also induces the phase noise on the VCDL output phase that is also verified using the HSPICE simulations. The phase noise appears as skirt on the spectral line of the fundamental frequency.

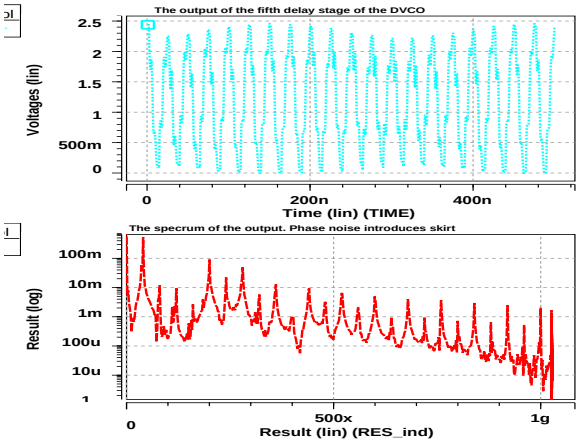


Fig. 6. (a) The output voltage in the presence of the substrate noise. (b) the output spectrum

Now, to quantify the VCDL phase noise and the DLL jitter induced by the substrate noise, we first obtain the VCDL phase noise in response to the substrate noise variations. For the ultimate design criteria of having a small coupling from the substrate and the supply to the DLL circuit we can simplify the Eq. (6) and derive the autocorrelation function of the excess frequency variations in terms of the autocorrelation of the substrate noise. Utilizing Eq. (6) and doing some trivial calculations the current variations due to the substrate noise is roughly equal to:

$$\Delta I_{SS,noise} = W\upsilon_{sat}C_{ox}(1-\kappa^2)v_{sub} \quad (7)$$

where v_{sub} accounts for the total contributions of the coupled noise on the control line and coupled noise through the substrate bulk. Interestingly, according to Eq. (7) the short-channel transistors have less noise contribution on the drain current fluctuations than the long-channel transistors which is in agreement to the physical description of the substrate noise effect on transistor current. This current variation directly affects the VCDL output phase as follows:

$$\Delta\Phi_{VCDL} = \frac{2\pi N}{T_{clock}} \frac{W \upsilon_{sat} C_{ox} (1-\kappa^2)}{C_L V_{DD}} v_{sub} = K_{VCDL,noise}\, v_{sub} \qquad (8)$$

where C_L is the total load capacitance including the capacitances seen looking at the input terminal of the following stage, the diffusion capacitances of the current delay stage, and other non-parasitic physical load capacitances. Eq. (9) is used to obtain the autocorrelation of the frequency variation and subsequently the power spectral density of the VCDL phase variations.

$$S_{\Phi_{VCDL}}(\omega) = K^2_{VCDL,noise}\, S_{sub}(\omega) \qquad (9)$$

where $S_{sub}(\omega)$ is the spectral density of the substrate noise and is given by Eq. (2-b). As a consequence, the simplified linear relationship between the substrate noise and the incremental current variation of the current tail allows one to consider the effect of the substrate noise as an additive noise in the closed-loop system. In a robust DLL circuit with a larger than required lock-range, the VCDL phase noise induced by the substrate noise causes the timing jitter at the output without making the DLL loop to become unlocked. Therefore the timing jitter in response to the VCDL phase noise is obtained under the locked condition. The closed-loop DLL system is a linear feedback system under the locked condition and the power spectral density of the output is related to the spectral density of the VCDL phase variations by the squared magnitude of the closed-loop transfer function:

$$S_{\Phi_{DLL}}(\omega) = |H_{DLL}(\omega)|^2 S_{\Phi_{VCDL}}(\omega) = \left| \frac{1}{1 + (I_P/(2\pi)) H_{LP}(\omega) K_{VCDL,noise}} \right|^2 S_{\Phi_{VCDL}}(\omega) \qquad (10)$$

where $H_{LP}(\omega)$ is the loop filter, and I_P is the constant current source in the charge-pump circuit. $S_{\Phi_{VCDL}}(\omega)$ is the power spectral density of the excess phase induced by the substrate noise coupling whose power spectral density is given by Eq. (9).

The main source of the substrate noise is from the fast digital transients of the digital circuits. Since the dominant component of the substrate noise injection in large-scale digital blocks is from the power/ground bounce across a highly inductive chip-package interface, the substrate noise is similar to periodic spikes. Therefore the noise expression in Eq. (1) is simplified to an impulse train. The power spectral density of the substrate noise becomes:

$$\tilde{S}_{sub}(\omega) = \frac{1}{T}[\, S_{A_{sub,N}}(e^{j\omega}) + S_{A_{sub,P}}(e^{j\omega})] \qquad (11)$$

Recall that $A_{sub,N(P)}$ is a discrete-time random process that accounts for the number of adjacent switching circuits switching simultaneously. The number of adjacent switching circuits is uncorrelated to the number of adjacent switching circuits in another circuit location. Therefore the random amplitude of the noise spikes, $A_{sub,N(P)}$, is modeled as white noise process with total average power of $\overline{A^2_{sub,N(P)}}$. The phase-noise of the DLL output phase and the timing jitter is easily derived using equations (2-b), (9), and (10). As a special case of having a narrow-band loop filter made by series R_p-C_p circuit, the equations for the power spectral density and the DLL timing jitter have a simple form as follows:

$$\tilde{S}_{\Phi_{DLL}}(\omega) = \frac{\overline{A^2_{sub}}}{T} \left(\frac{K_{VCDL,noise}}{1 + \frac{I_P}{2\pi} R_p K_{VCDL,noise}} \right)^2 \left(\frac{\omega^2}{\omega^2 + p_1^2} \right) \qquad (12)$$

where p_1 is the pole of the closed-loop DLL system and is equal to:

$$p_1 = \frac{\frac{I_p}{2\pi} K_{VCDL,noise}}{C_P + \frac{I_p}{2\pi} R_p C_P K_{VCDL,noise}}$$

According to the definition given in [9], the accumulated jitter is the standard deviation of the timing uncertainty. The variance of the timing jitter is thus equal to:

$$j^2_{\Phi_{DLL}}(\tau) = \frac{\overline{A^2_{sub}}}{2T} \left(\frac{K_{VCDL,noise}}{1 + \frac{I_P}{2\pi} R_p K_{VCDL,noise}} \right)^2 p_1 (1 - e^{-p_1|\tau|}) \qquad (13)$$

Examining Eq. (13) leads us to an important unique observation with regard to DLL circuits. The jitter due to the substrate noise in a CMOS DLL is diminished by using a narrow-band DLL. Consequently, DLL circuits exhibit a better jitter performance compared to the PLL circuits.

To verify the closed-form expressions given by equations (12) and (13), ten inverters are connected to the same voltage and ground lines as the DLL. The drivers switch simultaneously, and the jitter of the DLL due to the substrate noise is simulated. Table 1 shows a comparison of the phase noise levels of the DLL using Eq. (12) with the simulated results. Compared to the simulations, the results are very close in the frequency range where the VCDL phase noise is dominant. This shows the validity of our VCDL phase noise formulations.

Table 1: Comparison between the simulated and the measured results

Frequency offset (kHz)	Analytical [dB/Hz]	Simulation [dB/Hz]
4.0	-64.2	-63.8
8.2	-72.3	-71.2
13.0	-81.0	-80.2
21.0	-85.3	-84.3
33	-90.0	-89.4
48	-92.1	-91.0
65	-96.5	-95.8
90	-105.6	-104.8

4. CONCLUSIONS

In this paper we presented a study of the substrate noise effect in the DLL timing jitter. First, a new stochastic model for the substrate noise was proposed. This model was then utilized to study the clock jitter in clock generators that utilize the delay-locked loop (DLL) system. This paper presented a mathematical model for calculating the substrate noise-induced timing jitter in DLLs. The model relies on the stochastic representation of the substrate noise and its effect on the jitter of the VCDL and finally the timing jitter of the DLL. Experimental results demonstrate the accuracy of the analytical predictions compared to the measured results.

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