Analysis and Reduction of Capacitive Coupling Noise in High-Speed VLSI Circuits

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Abstract-- *Scaling the minimum feature size of VLSI circuits to sub-quarter micron and its clock frequency to 2GHz has caused crosstalk noise to become a serious problem, that degrades the performance and reliability of high speed integrated circuits. This paper presents an efficient method for computing the capacitive crosstalk in sub-quarter micron VLSI circuits. In particular, we provide closed-form expressions for the peak amplitude, the pulse width, and the time-domain waveform of the crosstalk noise. Experiments show that our analytical predictions are at least two times better than the previous models in terms of the prediction accuracy. More precisely, experimental results show that the maximum error of our predictions is less than 10% while the average error is only 4%. Finally, based on the proposed analytical models, we discuss the effects of transistor sizing and buffering on crosstalk noise reduction in VLSI circuits.*

1. Introduction

Rapid advances in VLSI technology have enabled us to reduce the minimum feature sizes of VLSI circuits to sub-quarter microns and the switching times to tens of picoseconds or even less. Unfortunately, this comes at a cost. The digital circuits have now become subject to the same type of problem that analog integrated circuits have been affected by since their inception. That problem is noise. Although the device noise sources (i.e. shot noise, flicker noise, thermal noise) are still not an issue in the performance of digital circuits, external noise sources (i.e. crosstalk, power/ground bounce, substrate noise) significantly degrade the performance and the reliability of digital integrated circuits. These external noise sources are mostly due to the fact that on-chip interconnects act like transmission lines where the neighboring wires exert electric and magnetic couplings on each other. Among the various external noise sources, problems related to the on-chip capacitive crosstalk are particularly important. Because the thickness of the wires is not scaled down as much as the width of the wires is and because the wires are packed increasingly closer together, the interwire coupling capacitances become larger, the ratio between the coupling capacitance and the total capacitance increases, and as a result the capacitive coupling noise increases. High-speed digital circuits heavily use the dynamic logic family. Dynamic circuits with their two phase of operations are more susceptible to crosstalk noise compared to the static logic circuits.

Various techniques can be utilized to estimate the crosstalk noise. The most accurate but very time consuming approach is to use HSPICE simulation. For example, our experiments show that simulating a small circuit (e.g., a collection of five coupled lossy transmission lines) with HSPICE takes almost three minutes on a 866MHz Intel processor. Since the interconnects are modeled as linear time-invariant systems, model reduction techniques [1][2][3][4][5] can be utilized to reduce the computational complexity. However, model reduction techniques, although helpful, do not adequately solve the problem of long computation times. In addition, these techniques do not provide any insight to the circuit designers as how to modify the circuit structures in order to reduce the crosstalk noise.

Deriving simple closed-form expressions that can predict noise behavior is more desirable than running a simulation tool. This is especially true during the early stages of the design process when one cannot afford to simulate a large number of possible circuit structures and layout solutions. Consequently, a number of researchers have tackled this problem. Vittal *et al.* in [6] provide bounds for the crosstalk noise using a lumped RC model, but this work ignores the interconnect resistance. Later on, the same authors, in paper [7], use the geometrical properties of the crosstalk noise to obtain expressions for the peak amplitude of the noise as well as the noise pulse width. Their techniques can handle arbitrary input signals. Devgan in [8], proposes a simple yet clever approach to find an upper bound for crosstalk noise. The author himself mentions that his model exhibits a large error when the signals are fast and the rise and fall times are short. Unfortunately, this latter scenario occurs frequently when practical values of the interconnect parasitics and signal frequencies are used. We have observed that the percentage of the estimated error in such cases can be as much as 60%. In addition, Devgan [8] does not predict the noise pulse width. Knowing the noise pulse width is important because, in general, the noise margin of a gate depends on both the noise amplitude and pulse width.

In this paper we propose a new crosstalk noise metric that is capable of predicting the noise amplitude and noise pulse width of an RC interconnect as well as an overdamped RLC interconnect. Our noise metric has a closed form expression that clearly specifies the dependency of the noise on the aggressors and victim line circuit parameters as well as the rise/fall times. We then use our metric in two commonly-used noise reduction techniques to calculate relevant characteristics of the line drivers and buffers.

The remainder of the paper is organized as follows. In section 2, capacitive coupling is reviewed, and through experimental results, it is shown that the inductive coupling on chip is negligible for local wiring clocked at a target frequency of 500MHz. After a brief description of Devgan's metric, we introduce our noise metric. We compare our metric with the results of Vittal [7] and Devgan [8] in a series of detailed experiments. In section 3 we introduce a technique to reduce crosstalk, and we show how our metric can be suitably fitted to this noise reduction technique. Section 4 has our concluding remarks.

2. Capacitive coupling

As circuit speeds increase, the effects of on-chip crosstalk noise become more pronounced. Fig. 1 shows N neighboring wires. The high frequency operation of VLSI circuits causes the on-chip wires to exhibit transmission line effects, and hence we have electrical and magnetic couplings between any pair of wires. These electric and magnetic couplings reshape the signal waveforms and potentially induce delay in the signals traveling through the lines.

Fig. 1. Circuit schematic of N on-chip interconnects

Fig. 2 depicts five microstrip lines powered by five CMOS drivers along with their distributed RLC circuit model. The geometrical parameters of the lines and device sizes are shown in the figures. The wire lines and the shieldings are all in copper. The input to the first, second, and fourth lines are periodic square waveforms with non-zero rise and fall-times of 80 *psec*. The third and fifth lines are held steady with a high input voltage at the input of the first driver and the fifth driver. The cycle-time is 2nsec. Fig. 3 indicates a tightly coupled distributed RLC model that is used to model N electromagnetically coupled interconnects (for our example, $N = 5$).

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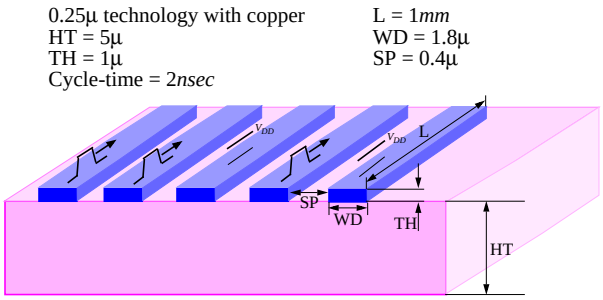


Fig. 2. Five parallel microstrip lines in 0.25μ CMOS technology

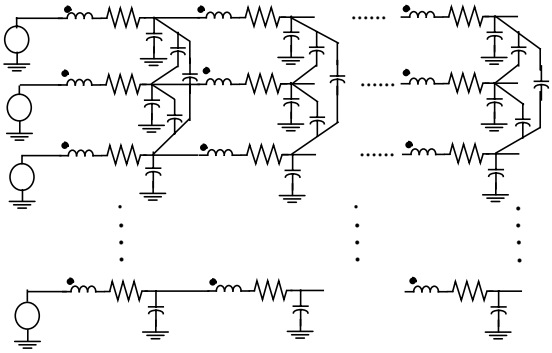


Fig. 3. Circuit schematic of N interconnects that are eletromagnetically coupled to each other

For the interconnect circuit in Fig. 2, HSPICE simulation shows that the resistance value is more than ten times greater than the impedance represented by the inductance at 2*nsec* clock cycle time. Therefore, the distributed RC circuit representation is used instead of the more accurate distributed RLC representation. To verify this simplification, the following experiment is performed:

First, the distributed RLC circuit that was extracted from the HSPICE output file is used. The simulation is run on this circuit to determine the noise waveform. In the next step, inductances are set to zero, and the simulation is run again on this new circuit. Fig. 4 shows the results of these simulations on the circuit shown in Fig. 2. From Fig. 4, we see that the noise waveforms of the two circuits are the same and that we cannot distinguish these two waveforms in the figure. The absence of any ringing at the output voltage of the interconnect (with a 2*nsec* clock cycle time) validates the assumption of modeling the interconnect with distributed RC circuits only.

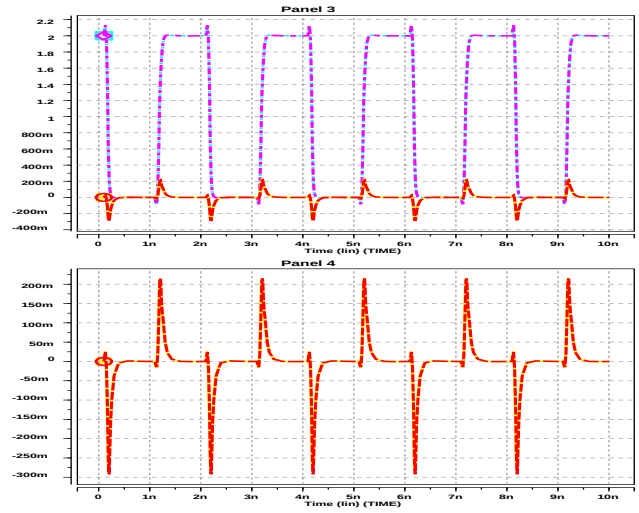


Fig. 4. Comparison between the distributed RC circuit model and the RLC model of Fig. 2 using the HSPICE simulation

From Fig. 4 we see that for local wires the on-chip capacitive coupling is more pronounced than the on-chip inductive coupling. Therefore, in this paper, we focus on the capacitive coupling noise problem.

Our goal is to develop a circuit model to predict the capacitive coupling for on-chip coupled interconnects and thereby derive a closed-form expression for the crosstalk noise. We start our analysis by reviewing the derivation of Devgan's metric and its drawbacks in estimating the crosstalk noise in RC circuits. For a more comprehensive explanation of this metric, please refer to [8].

2.1. Devgan's metric for crosstalk noise estimation

Consider two capacitively coupled RC networks as shown in Fig. 5.

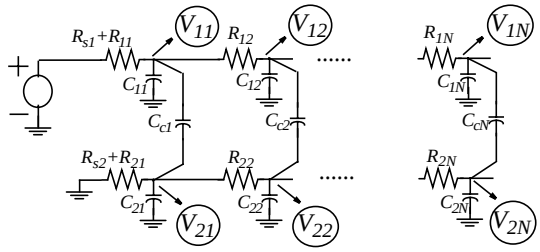


Fig. 5. Circuit schematic of capacitively coupled aggressor and victim nets

One RC ladder network (called the *aggressor* net) is driven by a flattened ramp voltage whereas the second RC ladder (called the *victim* net) is quiet. For this circuit, the node voltage vector at the victim net, $\mathbf{V}_2 \in \Re^{N\times 1}$, is related to the voltage vector at the aggressor net, $\mathbf{V}_1 \in \Re^{N\times 1}$, through the following equation:

$$[(s\mathbf{C}_2 - \mathbf{A}_{22}) - s\mathbf{C}_c(s\mathbf{C}_1 - \mathbf{A}_{11})^{-1}s\mathbf{C}_c]\mathbf{V}_2 = -s\mathbf{C}_c(s\mathbf{C}_1 - \mathbf{A}_{11})^{-1}\mathbf{B}_1\mathbf{V}_s \quad (1)$$

where $\mathbf{C}_i = diag(C_{ij} + C_c)$ for i = 1, 2 and j = 1, 2, . . ., N and $\mathbf{C}_c = diag(-C_{cj})$ for j = 1, 2, . . ., N. $\mathbf{A}_{11}$ and $\mathbf{A}_{22}$ represent the equivalent node resistance matrices of the aggressor net and the victim net, respectively. Given an infinite ramp input, the node voltages at the victim node monotonically increase toward their final values. Hence, the voltage values at $t = \infty$ are indeed the largest possible values of node voltages at the victim net. The *final value theorem* is utilized to determine the steady-state values of node voltages at the victim net. The result is:

$$\mathbf{V}_{2,ss} = -\mathbf{A}_{22}^{-1}\mathbf{C}_c\mathbf{A}_{11}^{-1}\mathbf{B}_1\frac{V_{DD}}{t_r} \quad (2)$$

where t_r is the rise-time of the input signal. For simplicity, it is assumed that the rise and fall times are equal. Note that this result is valid only if the driving voltages of the interconnects are infinite ramps. This is a critical assumption that seriously limits the accuracy of capacitive crosstalk estimation. In practice, the actual driving voltages of the interconnects are saturated ramp inputs rather than infinite ramps. This means that the node voltages at the victim net reach their peak value at $t = t_r$. This peak value is obviously different from the steady-state value under the infinite ramp input, and the error between these two values can be quite large if the rise-time of the input is fast.

To better understand the shortcoming of this approach, consider two second-order RC circuits with two floating capacitances connecting the corresponding nodes of these two circuits. The circuit structure is shown in Fig. 6.

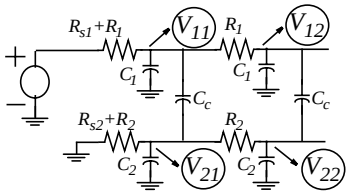


Fig 6. A pair of capacitively coupled second-order RC circuits coupled through floating capacitance, C_c

According to the HSPICE simulation, the reported peak value of voltage V_{22} is 0.505*V*. Devgan's metric for two coupled RC sections yields the following equations:

$$V_{21,ss} = 2(R_2 + R_{s_2})C_c\frac{V_{DD}}{t_r} \quad (3)$$

$$V_{22,ss} = (2R_2 + 3R_{s_2})C_c\frac{V_{DD}}{t_r} \quad (4)$$

Using Eq. (4), $V_{22,ss}$ is 0.75V. The estimated error is 48.5%. Since the rise-time is small, the crosstalk waveform rolls down quickly, and as a result, the error becomes unacceptably large (see Fig. 7). For cases where the rise-time is large compared to the interconnect delays, Devgan's metric can accurately predict the peak value. Unfortunately, cases in which the estimations are accurate (i.e., the slow slew-time

for the pulses), are unimportant from a circuit performance viewpoint. The reason is that the peak value of the crosstalk is inversely proportional to the input rise-time. For slow slew waveforms, the crosstalk also has a small peak value and thus has little effect on the circuit delay and logic failure rate.

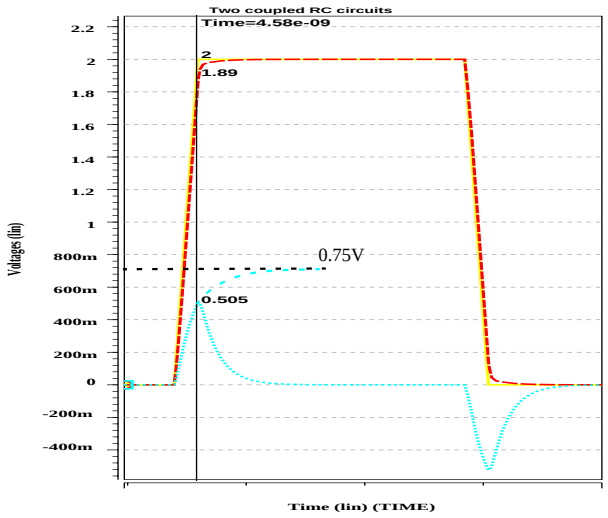


Fig. 7. The output voltage and the crosstalk of two coupled second-order RC circuits. C_1 = 60fF, C_2 = 120fF, R_2 = 100, R_1 = 20, C_c = 100fF, t_r = 0.08ns

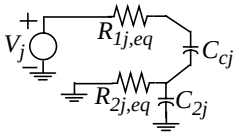
In the next section we derive a new, more accurate noise metric and compare our results with Devgan's results and with HSPICE simulations.

2.2. A new metric for crosstalk noise estimation

Examining the HSPICE results reported in Fig. 7 helps us identify one source of inaccuracy in Devgan's metric. The large error in this example comes from the fact that the time constants of the exponentially rising portions of victim node voltages, V_{2j} for j = 1, 2, . . ., N, in the circuit of Fig. 5 are comparable to (or larger than) the input rise time. The actual peak value of the crosstalk occurs approximately at $t = t_r$. To compute this peak value, we recognize that the capacitive crosstalk noise at every node of the victim net is a rising exponential function in the input transient interval. The actual peak value of the crosstalk noise at every node of the victim net is the value of the corresponding rising exponential function at $t = t_r$ where the steady-state value of this exponential function is determined by Devgan's metric.

$$\mathbf{V}_{2,max} = \mathbf{V}_{2,ss}\left(\mathbf{I} - \mathbf{exp}\left(\mathbf{diag}\left(-\frac{t_r}{\tau_{d_j}}\right)\right)\right) \qquad \text{for } j = 1, 2, ..., N \qquad (5)$$

where **diag**(.) represents the diagonal matrix. τ_{d_j} is the time constant of the j-th node voltage in the victim net, and $\mathbf{V}_{2,ss}$ is the vector of steady state values of the crosstalk noise voltages at the victim nodes as calculated from Devgan's metric. Each node in the victim net sees two capacitances: a grounding capacitance, C_{2j}, and a floating coupled capacitance, C_{cj}. The time constant at each victim node is thus proportional to the time constants seen across each of these two capacitances. To accurately estimate this time constant, we first construct an equivalent circuit consisting of C_{2j}, C_{cj}, and the equivalent resistances seen across these two capacitances and replace all of the other capacitances with open circuits. This circuit model is shown in Fig. 8.



$$R_{1j,eq} = \sum_{i=1}^{j} R_{1i}$$

$$R_{2j,eq} = \sum_{i=1}^{j} R_{2i}$$

Fig. 8. The equivalent circuit for computing the time constant of the j-th node of the victim net

The characteristic polynomial of this second-order transfer function is:

$$\Lambda_j(s) = R_{1j,eq}R_{2j,eq}C_{2j}C_{cj}s^2 + \overbrace{[(R_{1j,eq}+R_{2j,eq})C_{cj}+R_{2j,eq}C_{2j}]}^{\tau_{v_j}}s + 1 \qquad (6)$$

The time constant of this second-order circuit, which is roughly the inverse of the 3-dB bandwidth of its system transfer function, is equal to the coefficient of the first-order term, named τ_{v_j}. As a result, τ_{d_j} should contain this coefficient as a part of its expression. However, it should be noted that the input voltage source is assumed to be a unit step function for τ_{v_j} to properly represent the time constant at the j-th node of the victim net. This is obviously not the case for the coupled RC circuits. The input voltage to the j-th node of the aggressor itself experiences an RC delay due to the existing RC path from the input to the j-th node. This RC delay also needs to be accounted for. In addition, for RC circuits with orders greater than one, the initial slope of the step and ramp responses is zero. This zero initial slope leads to an increase in the circuit delay. Fig. 9 indicates all these delay effects on crosstalk noise under a flattened ramp input as is compared with the crosstalk noise under a step input.

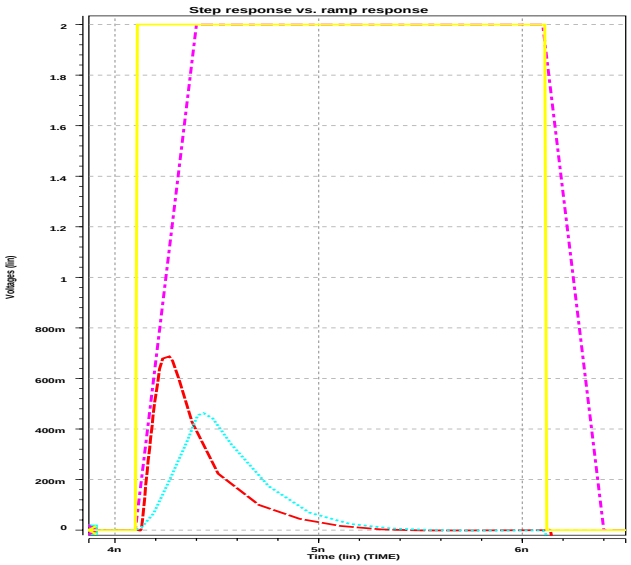


Fig. 9. Effects of zero initial slope and RC delay on the crosstalk

Consequently, the time constant of the j-th node in the victim net consists of two additive terms τ_{v_j} and τ_{a_j}, where τ_{v_j} represents the time constant of the j-th node in the victim net under a unit step input excitation, and τ_{a_j} represents all additional delays as explained above.

$$\tau_{d_j} = \zeta\cdot[(R_{1j,eq} + R_{2j,eq})C_{cj} + R_{2j,eq}C_{2j} + \tau_{a_j}] \quad \text{for } j=1, 2, ..., N \quad (7)$$

where τ_{a_j} is:

$$\tau_{a_j} = R_{1j,eq}(C_{cj} + C_{1j}) + \sum_{k=1}^{j-1}[R_{1k,eq}(C_{ck} + C_{1k}) + R_{2k,eq}C_{2k}]$$

for $j=1, 2, ..., N$ (8)

and ζ is a constant factor for the delay increase due to the nonzero finite input slope. Its value is in the range [1.05 , 1.1]. Throughout our analysis we will assume that $\zeta = 1.07$. As can be seen, the peak amplitude of the crosstalk is easily obtained by these calculations.

To measure the level of accuracy that can be obtained by our metric, the peak crosstalk noise of two coupled second-order RC sections with different values for the input rise-time and RC values is computed and the results are compared with those obtained by HSPICE simulation as well as by Devgan's metric. Our new metric yields the following equations for the two capacitively coupled second-order RC circuits depicted in Fig. 6:

$$V_{21,max} = V_{21,ss}\left(1 - \exp\left(-\frac{t_r}{\tau_{d_1}}\right)\right) \qquad (9)$$

where

$$\tau_{d_1} = 1.07[(R_1 + R_{s1})(2C_c + C_1) + (R_2 + R_{s2})(C_c + C_2)]$$

$$V_{22,max} = V_{21,ss}\left(1 - \exp\left(-\frac{t_r}{\tau_{d_2}}\right)\right) \qquad (10)$$

where

$\tau_{d_2} = 1.07[(2R_1 + R_{s1})(C_c + C_1) + (2R_2 + R_{s2})C_2 + (R_1 + R_2)C_c]$

The supply voltage is V_{DD}=2*V*, and the cycle-time is 2*nsec*. Table 1 contains the results of these comparisons. In Table 1 the source resistances are assumed to be zero.

To verify the accuracy of our approach on multistage RC stages and also to compare with other expressions proposed in [7] and [8], we set up a set of experiments on a two-line structure in 0.25μ*m* CMOS technology. The coupling lengths of the adjacent interconnects are varied from 100μ*m* to 2*mm*. Results are compared for a range of rise-times varying between 30*ps* and 200*ps*. Table 2 contains the result of these comparisons. The mean and maximum errors are reported in Table 3. These tables demonstrate the higher accuracy of our approach compared to the two previous noise expressions reported in [7] and [8].

The susceptibility of logic gates to noise depends not only on the peak amplitude of the crosstalk noise but also on its duration. For example, digital circuits can often tolerate (and indeed filter out) spike-like crosstalk noise with a large peak amplitude and very small noise pulse width. Furthermore, in static logic circuits, the peak amplitude of crosstalk does not result in loss of signal values. Instead, it tends to cause an increase in propagation delay along the victim line (which in turn may cause setup time violation in high-speed circuits). These observations create the necessity for determining the complete noise waveform.

Given the equivalent time constant and the peak amplitude of the crosstalk, the noise waveform can be calculated by the following equation:

$$\boldsymbol{v}_2(t) = \begin{cases} \mathbf{V}_{2,ss}\left(\mathbf{I} - \mathbf{exp}\left(\mathbf{diag}\left(-\frac{t}{\tau_{d_j}}\right)\right)\right) & 0 \le t \le t_r \\ \mathbf{V}_{2,max}\ \mathbf{exp}\left(\mathbf{diag}\left(-\frac{t-t_r}{\tau_{d_j}}\right)\right) & t \ge t_r \end{cases} \quad \text{for } j = 1, 2, \ldots, N \tag{11}$$

Please note that having the noise waveform gives us the maximum amount of information regarding the noise behavior including the peak amplitude of crosstalk noise as well as the noise pulse width. This information allows designers to find better solutions for noise avoidance.

Fig. 10 compares Eq. (11) with HSPICE simulation for a pair of capacitively coupled nets. As one can see, the new metric can accurately predict not only the noise peak amplitude but also the noise pulse width. Indeed, the effective pulse width is estimated within a 5% error.

Our metric is easily utilized for the general case of having several parallel runs of on-chip interconnects at the same and/or other layers of metal by using the superposition principle.

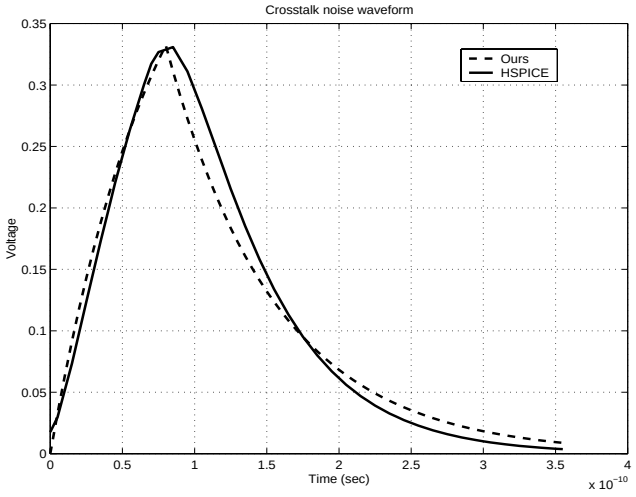


Fig. 10. Crosstalk noise waveforms for two coupled transmission lines. The line characteristics are given as the last entry of Table 2

Fig. 11 shows the change in crosstalk when the input rise time varies from 50*ps* to 300*ps* and all the geometrical parameters are fixed. Comparing HSPICE with our approach confirms that one achieves a high accuracy with our noise metric over a wide range of input rise-times. As expected, for long rise-times Devgan's metric accurately predicts the peak amplitude of the noise. Vittal's metric produces higher fidelity results compared to Devgan's, its estimation error remains roughly constant, and it does not have as large a dynamic range as Devgan's. In paper[7], the authors use geometric arguments to come up with crosstalk noise expression. As a result, they do not account for the effects of the non-ideal delays on the crosstalk peak estimation. On the contrary, our metric is based on the actual characteristics of capacitvely coupled RC circuits that are derived from several simulations. Consequently, our metric is more accurate than the works in papers [7] and [8].

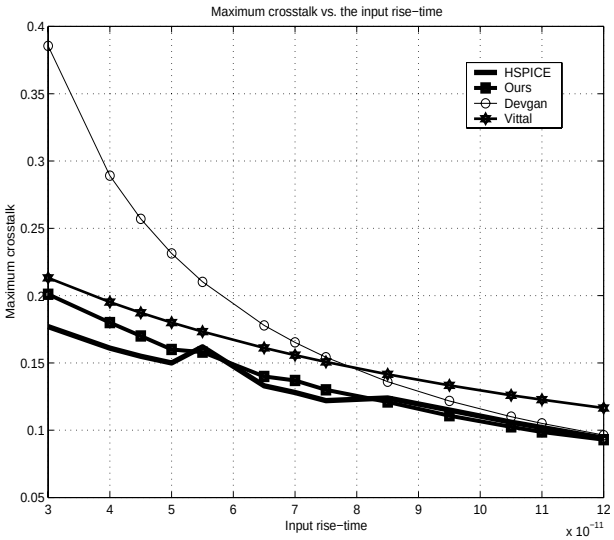


Fig. 11. Maximum crosstalk noise vs. input rise-time

3. Use of a Schmitt trigger circuit as a buffer

An effective circuit technique to filter out the crosstalk noise is to do buffer insertion. Alpert *et al.* in [10] show that buffer insertion is effective for simultaneous optimization of timing and noise. This paper, however, uses Devgan's metric for formulating the crosstalk noise constraint. As we saw in the previous section, this metric produces a large error for short input rise-times. An obvious improvement would be to use our new metric for capturing the noise constraints. Going further, using Schmitt trigger circuits instead of buffers provides us with the flexibility to adjust the switching threshold voltage according to the direction of the input signal transition as illustrated in Fig. 14 From a circuit modeling point of view, a Schmitt trigger operates like a resized inverter with $W_n >> W_p$ for a low-to-high transition at the input and with $W_p >> W_n$ for a high-to-low transition at the input. Notice that because of this adjustment to the switching threshold of the Schmitt trigger buffers, these buffers are less susceptible to the crosstalk noise, i.e., they can filter out noise pulses with a large peak amplitude.

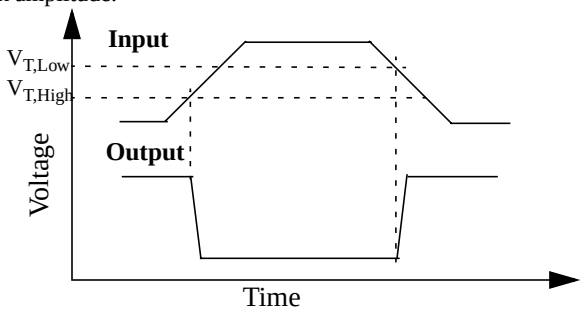


Fig. 14. Signal detection of a Schmitt trigger

To use a convenient circuit structure for the Schmitt trigger we should consider some important facts here:

1. The Schmitt trigger should compensate for the line delay. It should have as high a gain in transition response as an inverter with the corresponding gate size.

2. The Schmitt trigger should operate correctly in sub quarter micron CMOS technology with low supply voltage in the range of 1.3V-1.8V. As a consequence, the circuit structure should not contain stacked transistors. Given the above facts, we use the circuit structure

shown in Fig. 15.
The ratio of gate aspect ratios of transistors MN_1 and MN_2 are used to define the lower and upper threshold voltages of the Schmitt trigger. The operation of this Schmitt trigger is described next.

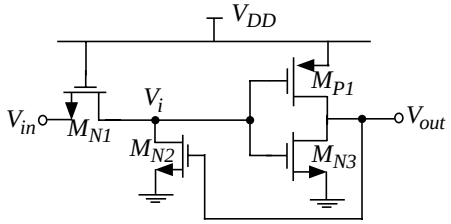


Fig. 15. The Schmitt trigger circuit used for filtering the crosstalk

Suppose that the input is initially low ($V_{in} = 0V$). Transistors MN_1 and MN_2 are in their linear regions, and the voltage V_i is obtained by a resistive voltage division from the input voltage. The output voltage is in the high logic state. As the input voltage increases, voltage V_i also increases at a lower rate due to the RC time constant seen at this node. When V_i reaches the threshold voltage of the NMOS transistor MN_3, the logic switching occurs. The positive feedback across the inverter that is produced by MN_2 causes a very fast transition time at the output. The threshold voltage for the high-to-low transition at the output is thus equal to:

$$V_{THL} = V_{tn}\left(\frac{r_{DS_2} + r_{DS_1}}{r_{DS_2}}\right) \tag{12}$$

The same analysis is performed for the low-to-high transition at the output, with the exception of having the threshold voltage of MP_1 as the point where the low-to-high logic switching occurs. The threshold voltage for the low-to-high transition at the output is thus equal to:

$$V_{TLH} = V_{DD} - V_{tn,body} - |V_{tp}| \tag{13}$$

where r_{DS_1} and r_{DS_2} are the on-resistance of transistors MN_1 and MN_2 respectively. $V_{tn,body}$ is the threshold voltage of MN_1. Fig. 16 shows the input and output waveforms of the Schmitt trigger circuit, with the gate aspect ratios depicted in the figure.

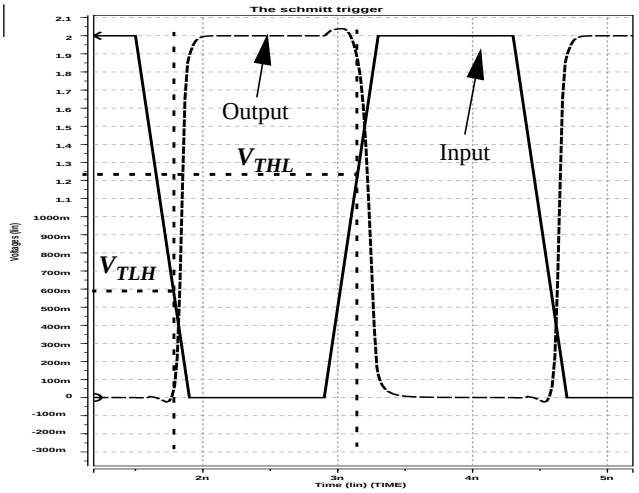


Fig. 16. Input and output waveform of the Schmitt trigger shown in Fig. 15

The noise waveform and particularly the peak value of crosstalk noise given by Eq. (5) is a function of the driving circuit and the load circuit impedances. To clarify this statement, let us assume that the distributed elements of each interconnect are all the same:

$$R_{1i} = R_{1j} = R_1 \ , \ C_{1i} = C_{1j} = C_1 \qquad \text{for all } i, j \in \{1, \ldots, N\}$$

$$R_{2i} = R_{2j} = R_2 \ , \ C_{2i} = C_{2j} = C_2 \qquad \text{for all } i, j \in \{1, \ldots, N\}$$

and that all of the coupling capacitances are the same:

$$C_{ci} = C_{cj} = C_c \qquad \text{for all } i, j \in \{1, \ldots, N\}$$

Under these assumptions, Eq. (7) is simplified to the following equations:

$$\tau_{d_N} = \zeta \cdot [\tau_{R_1} + \tau_{R_{s1}} + \tau_{R_2} + \tau_{R_{s2}}] \tag{14}$$

where

$$\tau_{R_1} = \left[\frac{N(N+3)}{2}C_c + \frac{N(N+1)}{2}C_1 + NC_{L1}\right]R_1 \tag{15}$$

$$\tau_{R_{s1}} = [(N+1)C_c + NC_1 + C_{L1}]R_{s1} \tag{16}$$

$$\tau_{R_2} = \left[NC_c + \frac{N(N+1)}{2}C_2 + C_{L2}\right]R_2 \tag{17}$$

$$\tau_{R_{s2}} = [C_c + NC_2 + C_{L2}]R_{s2} \tag{18}$$

R_{s1} and R_{s2} are the output resistances of the Schmitt trigger circuits driving the aggressor and victim lines, respectively. Using equations (14)-(18) along with equations (12) and (13), we can find the (W/L) ratios of transistors in the Schmitt triggers. Due to the high accuracy of the noise expressions, we can find optimal transistor sizes for maximum noise reduction.

4. Conclusions and Future Works

In this paper, we presented an efficient analysis technique for the capacitive crosstalk computation in sub-quarter micron VLSI interconnects. We derived closed-form expressions for the peak amplitude, the pulse width, and the time-domain waveform of crosstalk noise. Experiments show that our technique is at least twice as accurate as previous works. Experimental results show that the maximum error is less than 10% and the average error is 4%. We also briefly discussed sizing and buffering techniques for the noise reduction. We used our new metric as a noise calculation engine for these optimizations.

As mentioned before, the noise margin of a gate depends on both the noise amplitude and pulse width. Therefore the noise pulse width must also be taken into consideration in the circuit design for noise elimination. We will use our noise expressions for the peak amplitude and the pulse width to derive a new figure of merit that takes the effect of both the peak amplitude and noise pulse width into account. This figure of merit will give useful guidelines to optimally resize the buffers and Schmitt triggers for noise avoidance.

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Table 1. Comparison of the crosstalk noise computed by HSPICE, paper [8], and our metric

C_1 fF	C_2 fF	R_2	R_1	C_c fF	t_r ns	HSPICE volts	Devgan volts	Ours volts
50	60	100	100	30	0.05	0.216	0.36	0.229
60	60	100	100	30	0.4	0.045	0.045	0.044
70	70	300	50	50	0.1	0.533	0.9	0.547
70	60	80	70	50	0.3	0.08	0.08	0.08
100	120	80	70	90	0.3	0.143	0.144	0.141
100	120	80	40	60	0.1	0.25	0.288	0.235
100	120	100	40	60	0.09	0.291	0.4	0.311
100	120	70	30	100	0.08	0.39	0.525	0.389
120	70	30	100	100	0.08	0.144	0.225	0.131
60	120	100	20	100	0.08	0.505	0.75	0.53
80	220	200	90	160	0.08	0.581	2.4	0.61
70	100	60	40	100	0.03	0.513	1.2	0.52

Table 2. The results of simulations on the 2 capacitively coupled transmission lines using star-HSPICE, paper [7], paper [8], and our metric

c_1 (pF/m)	r_1 (kΩ/m)	r_2 (kΩ/m)	c_2 (pF/m)	c_c (pF/m)	R_{s1}	R_{s2}	C_{out1} (pF)	C_{out2} (pF)	t_r nsec	L (mm)	HSPICE volts	Devgan volts	Vittal volts	Ours volts
88.47	11.47	11.47	89.47	54.36	500	150	0.3	0.05	0.03	0.1	0.0333	0.05457	0.0333	0.0362
94.1	9.55	9.55	94.1	62.43	80	30	0.2	0.06	0.04	0.7	0.0482	0.0732	0.0579	0.0512
97.87	9.55	9.55	97.87	78	20	40	0.3	0.1	0.03	0.8	0.129	0.1831	0.1589	0.1377
120	10.2	10.2	100	82	90	100	0.4	0.06	0.1	0.9	0.112	0.1547	0.1206	0.11
151	12	12	120	100	40	0.08	0.3	0.07	0.08	1	0.176	0.2158	0.2026	0.1798
170	15	15	170	120	20	30	0.2	0.1	0.15	1.3	0.0838	0.0837	0.1156	0.0825
200	17	17	190	155	20	10	0.3	0.05	0.07	1.6	0.129	0.172	0.162	0.133
235	20	20	220	200	15	20	0.05	0.1	0.12	2	0.236	0.2733	0.2546	0.2302
235	20	20	220	200	20	30	0.07	0.08	0.08	2	0.321	0.51	0.3325	0.3323

Table 3. Error comparison for three noise metrics

	%Error Devgan's	%Error Vittal's	%Error Ours
	63.4	21.6	8.7
	52	20.1	6.22
	41	23.2	6.7
	38	7.7	1.7
	22.6	15	2.15
	0.9	37.9	1.55
	33.3	25.6	3.1
	15.8	7.88	2.46
	58	3.58	3.52
Average	36.1	18.1	4.0
Maximum percentage error	63.4	37.9	8.7