Implementation of a Digital Timing Recovery Circuit for CDMA Applications

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Abstract— In this paper a novel timing tracking circuit for CDMA applications is presented. The circuit utilizes a linear interpolator and a Schmitt quantizer to achieve the optimal tradeoff between design complexity and robustness. System simulations, experimental measurements, gate counts and power consumption issues are presented and analyzed.

I. INTRODUCTION

Timing recovery systems are an integral and key part of any communication system. The design goal is to avoid or alleviate inter-symbol interference (ISI), by sampling the incoming waveform at the optimal instant in time (i.e., maximum eye opening). The timing recovery task is to extract the timing information from the received data and then use this information to adjust the frequency and phase of the local sampling clock. Timing recovery can be implemented in either analog or digital domains, however all digital timing techniques based on interpolation are preferred alternative to costly automatic correction loops that involve feedback to the analog section of the receiver [1].

Generally speaking, interpolation techniques can be used to interpolate among nonsynchronized samples to produce the correct strobe value at the output - i.e. as if sampling had occurred at the ideal instant. The function of the interpolation filter is to calculate one output sample \( Y(kT) \) at a time, using a set of adjacent input samples \( \{x(mT)\}_{m} \) and a fractional interval \( \mu \) where \( 0 \leq \mu \leq 1 \) is obtained from a timing control unit as shown in Figure 1. The generated samples \( Y(kT) \) can be expressed as:

\[
Y(kT) = x[(m_k + \mu_k)T_s]
\]

Figure 1 All digital timing tracking

The design criterion that varies depending on the application is “how accurate should the interpolation be” or rather what kind of digital processor is required to meet a specific signal to noise ratio. Furthermore, the design challenge is minimizing complexity while maintaining robustness, since typically these systems operate on samples that are several multiples of the Nyquist rate (2-4 times).

In this paper, we will discuss the design and implementation of an all-digital timing recovery circuit for WCDMA applications. Section II presents an overview of timing recovery in CDMA, while section III discusses the design considerations and tradeoffs to achieve a compact and yet robust system. System simulations that validate performance are presented and analyzed. In section IV, we present the VLSI implementation and describe the experimental setup used to validate performance; we will also present experimental measurements that indicate that the system meets target design goals. Finally, section V concludes the paper.

II. TIMING RECOVERY IN CDMA

Timing tracking in CDMA is typically performed using an early late timing error detector [1] to generate the fractional delay \( \mu \) proportional to the offset from the ideal sampling instant. Figure 2.a illustrates a raised cosine pulse which is the shaping pulse used for transmission in most CDMA applications. The ideal sampling point lies at the peak of the pulse as indicated in the figure. In an early-late circuit, (Pseudo-Noise) PN correlations are performed on both sides of the pulse. Since the pulse is symmetric, ideally the difference between the early and the late correlation will be equal to zero. However, as a timing offset occurs, the sign of this difference and it amplitude is an indication of the timing offset. Figure 2.b illustrates the characteristic “S” curve that represents the output of an early late circuit as a function of the timing offset.

A simplified block diagram of the proposed timing recovery system is depicted in Figure 3. In this system, a baseband signal is sampled by a free running ADC. The free running ADC has to be sampling at a minimum of the Nyquist rate. The sampled signal is then passed to an interpolator that interpolates to 8 samples per symbol. An 8x sampling rate provides the best tradeoff between sampling rate and timing granularity. The expected degradation due to residual 1/16th chip offset, \( \lambda \), can be estimated based on the analytical derivation in [2] as:

\[
P(E|\lambda) = \frac{1}{2} \left[ \text{erfc}(\sqrt{E/N_0}) + \text{erfc}(\sqrt{E/N_0(1-2|\lambda|)}) \right]
\]
The interpolator receives a fractional interpolation coefficient \( \mu \). The 8 samples per chip are presented to a “sample selection” block that selects the best on-time, early and late samples for correlation. A 512 chip correlation is performed on the pilot channel, where the difference between the early and late correlators is used to provide an indication of the timing offset. The on-time correlation is used to provide a coherent phase reference as shown by the multiplication of its conjugate with the error signal. Finally, the error signal is filtered and used to close the loop for both the sample selection and interpolator. In the remaining sections we will present a complete discussion of the design and performance tradeoffs required for robust operation.

III. DESIGN CONSIDERATIONS

A. Interpolator Design

The first block that we will specify is the interpolator where the following design criteria were investigated.

- Sampling rate at the interpolator input: (2x vs. 4x)
- Interpolator type: (Linear vs. Quadratic (Farrow[3]))
- Precision of the interpolation parameter \( \mu \)
  - 1 bit representing three states \( \{\mu=0,0.5,1\} \)
  - 2 bits representing five states \( \{\mu=0,0.25,0.5,0.75,1\} \)

To test the system, simulations were setup for two conditions. The first is a standard AWGN channel with fractional chip offset, while the second is a Rayleigh frequency selective fading channel as defined by the WCDMA standard case II (three multipath) [4].

Figure 4 illustrates the results for the AWGN case for an input sampling rate of 4x, a spreading factor of 4 and a timing offset of 1/8 of a chip duration. The power allocated to the pilot channel is -10 dB prior to de-spreading. It can be seen that there is very little difference in performance between a relatively complicated Farrow structure with 1 bit \( \mu \) and linear interpolators with 1 bit \( \mu \), which indicates that a good choice for AWGN channels to minimize complexity is a linear interpolator.

The system performance was then quantified in a multipath fading channel with parameters as described previously. Figure 5 presents the outage curves for the bit error rate for a spreading factor of 4 and a Pilot channel power level of -3 dB prior to de-spreading. The results again indicate that linear and quadratic interpolation performs almost identically for this scenario. An interesting observation to make is that linear interpolation with an incoming sampling of 4x and 1 bit for \( \mu \) performs almost exactly as a linear interpolator with 2 bits for \( \mu \) and an incoming sampling at 2x, and both are very close to the Farrow performance.

B. Control Loop Design

The system presented in Figure 3 can be further simplified as shown in Figure 6 where \( A \) represents the gain of the system, \( S \) represents the S curve generation with added noise due to the nature of the CDMA signal, \( H \) is the loop filter and \( Q \) is the quantizer used to quantize \( \mu \).
In order to achieve a truly hardware efficient structure, the loop filter was designed as a simple sign integrator. The loop bandwidth was simulated to converge at up to 20 ppm of frequency drift within 50-80 pilot symbols. Furthermore, a major simplification in the design is possible since one reference crystal is used for both RF and ADC sampling clock. This indicates that knowledge of the frequency offset can be directly incorporated in the timing loops to cancel the sampling clock frequency drift. The design can therefore be represented as shown in Figure 7, where \( f_{\text{off}} \) is the frequency offset and \( (E-L) \) is the output of the early late circuit. The timing correction value \( \Delta T_i \) can be expressed as follows:

\[
\Delta T_i = k_f \text{sign}(y_i) + k_f f_{\text{off}}
\]  

(2)

C. System Simulation

A system simulation was setup to test the architecture proposed in Figure 7. The simulation parameters are a Rayleigh fading channel with two multipath at a relative strength of -14 dB and 0 dB respectively with a separation of 3.7 \( T_c \) in time, where \( T_c \) is a chip duration of 260 ns. The timing offset is set to 0.25 \( T_c \). The incoming sampling rate is 4x and the number of bits for \( P \) is one using a linear interpolator. A frequency offset is introduced in the data stream set at 50 Hz with perfect frequency synchronization assumed. Finally, the SNR is set to -10 dB prior to de-spreading with 10 users actively contributing to the noise floor.

Figure 8 illustrates the convergence of \( \mu \) for the stronger multipath. It is interesting to note that convergence occurs after about 70 symbols, however after the loop converges there is significant oscillation in the quantized value of \( \mu \) as shown in the figure. This will degrade the overall SNR as well as increase power consumption.

The main point to note is that now the unquantized \( \mu \) does not converge to a fixed value but rather exhibits a low frequency oscillation. This is due to the fact that the Schmitt quantizer does not allow the circuit to revert back to a different sample until the Schmitt threshold is crossed. Even though this is forcing the unquantized \( \mu \) to remain in a non optimal point for a longer period of time, the stability of the quantized \( \mu \) leads to a better system performance. To validate this claim, we performed an ensemble of simulations for 300 different channel realizations and plotted the cumulative distribution function of the power observed on the difference between the early and late correlations after the loop has converged. Ideally, the power should be zero at optimal sampling, an increase in power indicates an increase in the value of the error. Figure 11 illustrate the results of this study showing that the use of the Schmitt quantizer improves the performance of the system by approximately 5 dB for a wide range of channel realizations.

IV. VLSI IMPLEMENTATION

The timing recovery circuit presented in this paper was implemented as part of a larger CDMA modem that can demodulate up to 20 multipath. The technology used is 0.18 \( \mu \)m CMOS with 1 poly layer and 6 metal layers. The supply voltage for the core is 1.8 v with 3.3 v for the pads. The frequency range of operation is 64-107 MHz.

Due to the architectural simplifications discussed, an extremely compact timing circuit was generated. Table 1 presents the area and NAND equivalent gates for the different parts of the circuit. Figure 12 depicts a die photo of the circuit.
fabricated chip with the location of different blocks identified. The (E-L) circuits are distributed throughout the ASIC as parts of the correlation banks (1 thru 4).

![Figure 11 Noise power in E-L loop](image)

Table 1 Area and gate count

<table>
<thead>
<tr>
<th>Sub-unit</th>
<th>Area (µm²)</th>
<th>Gates NAND Eq.</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interpolator</td>
<td>11 K</td>
<td>300</td>
<td>One (Shared)</td>
</tr>
<tr>
<td>(E-L) and filtering</td>
<td>24.4 K</td>
<td>650</td>
<td>One per multipath</td>
</tr>
<tr>
<td>Total Distributed</td>
<td>500 K</td>
<td>13,300</td>
<td>20 Multipath</td>
</tr>
</tbody>
</table>

![Figure 12 Entire modem die](image)

Experimental estimation of the power consumption is not trivial since by nature the circuit spans multiple blocks (interpolator, correlation banks, feedback filter etc.). For this reason a set of two tests were performed to isolate the power consumed. Table 2 presents a summary of the results. In the first scenario, the chip is running with one timing correction correlation activated as well as a pilot and a data channel. In the second test, no correlations are performed. The difference in power consumption between the two cases (14.9-8.3=6.6 mW) represents the incremental power required to demodulate and track (frequency and timing) one finger.

To determine the functionality of the circuit, it was tested using a Rayleigh fading channel emulator, using 20 ppm crystals in the receiver which translates to a possible frequency offset of ±20 KHz at a carrier frequency of 2 GHz.

Table 2 Power Consumption

<table>
<thead>
<tr>
<th>Scenario 1</th>
<th>Test</th>
<th>Chip running performing 3 correlators (1 Pilot, 1 Timing, 1 Data SF=16)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>14.9 mW</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Scenario 2</th>
<th>Test</th>
<th>Chip running performing zero correlations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>8.3 mW</td>
<td></td>
</tr>
</tbody>
</table>

Figure 13 illustrates the test setup used. The ADC sampling rate used is 15.36 MHz which is 4x the chip rate. The circuit successfully performed timing recovery and synchronization as indicated by the results shown in Figure 14 that depict the block error rate for a Rayleigh fading channel according to case 3 of the standard (4 multipath) for a data channel at 12.2 Kbps.

V. CONCLUSION

In this paper we presented a complete design of a timing recovery circuit for CDMA applications. Design tradeoffs have been presented and analyzed with the intention of implementing a low power compact and robust circuit. Experimental measurements validated system performance and robustness.

REFERENCES