Analysis of RF Flip-chip On-chip Inductance with Novel Measurement Technology

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\textit{Introduction}: Advances in integration technology and device performance require higher density packaging of high-frequency integrated circuits. Flip-chip technology is emerging as a leading technology to meet the high frequency and high-density requirements. Nowadays, the low cost of silicon IC’s compared to GaAs and the potential for integration with baseband circuits makes silicon the process of choice in many RFIC applications. However, silicon-based Integrated Circuit (IC) technologies have not been widely used with Flip-Chip (FC) technology for RF applications. Passive and active circuitries on flipped silicon die face different coupling and parasitics environment compared to the traditional wire-bond. Two major differences arise in the FC environment. The back plane of the die is no longer sitting on a ground plane. In addition, the top of the die faces ground plane that did not exist in the wire-bond applications. Since the introduction of inductor on lossy silicon, many papers have addressed on-wafer measure technique based on wire-bond packaging environment. However, conventional measurement approach to measure RF flip-chip faces some difficulties because conventional on-wafer technique can’t measure different electric and magnetic field effects that come from flip-chip configuration. The development of characterization technique for flip-chip packages is motivated by the need to predict the passive/active behavior of flipped environment at RF frequencies.

\textit{Inductor in Wirebond and Flip-chip Environment}: The location of the ground plane impacts the RF return path. Displacement and conduction currents into the substrate lead to the electromagnetic field losses in Si substrate. The inductor RF return path for flipped Si substrate is only associated with locations of ground substrate contacts that exists on the top surface of the die as well as ground on the package substrate. However, the inductor RF return path in wirebond package is associated with location of substrate contacts and die backside ground plane. This should also have an effect on the electromagnetic loss associated with On-chip inductance. In flip chip configuration, the top of the die faces the FC ground plane. This will also create eddy current in ground plane, which can lead to reduction in the effective inductance value in FC
configuration compared to wirebond. The analyzed flip-chip inductor uses same geometrical characteristics of the wirebond inductor except the lack of backside metal. The analyzed flip-chip inductors include bump height of 80 µm and underfill of $\varepsilon_r = 3.8$ between top package substrate ground and flipped inductor. The effective inductance of the FC inductor is larger than the wirebond inductor above 7 GHz. This can be explained by the eddy current effects associated with each configuration. The eddy current in Si substrate, which is stronger in the wirebond case, effects, appears at high frequency above 7 GHz for the structure under consideration. However, the eddy current in the ground plane of the FC configuration, which represents the RF return path exists at all frequencies, so the effective inductance for FC inductor is lower than the wirebond inductor at frequency below 7 GHz. The quality factor of flip-chip inductor is lower than the wirebond case due to lower effective inductance at low frequency and higher parasitic capacitance at high frequency as well as eddy current loss, as previously explained.

Structure of On-strip measurement: The RF flip-chip characterization technique using on-strip measurement method is developed. To measure the electric and magnetic characteristics of the flipped circuits, the die is mounted onto a package substrate. The transition structures of Ground-Signal-Ground (GSG) probes to on-chip spiral inductor on die are fabricated on low cost package substrate to measure the high-frequency response of RF flip-chip. In this technique, on-wafer measurements are applied to obtain S-parameters of mounted RF flip-chip. Transition between the Coplanar Waveguide (CPW) probe pads and the substrate Via is accomplished using tapered CPW traces under the package substrate. By modeling transition as a tapered CPW transmission line, the entire structure is designed to reduce reflection loss. Tapered CPW traces between substrate Via and bumps are located upper package substrate. Tapered CPW trace was optimized to reduce return loss and insertion loss using EM full-wave simulation, HFSS. Advanced Design Systems (ADS) was used to design optimized CPW probe pads. The structure of novel on-strip measurement method will be shown in conference.

Summary: In this paper, we analysis on-chip spiral inductor with RF flip-chip environment. We propose an on-strip technique to measure the RF performance of flipped die environment. By using new on-strip measurement technique, the effects of RF flip-chip environment can be measured easily. The new on-strip measurement structure is analyzed by the 3-D full electromagnetic simulation and experimentally characterized using vector network measurement and Ground-Signal-Ground (GSG) on-wafer probe station.