



CODES+ISSS 2003 Final Program

updated October 1, 2003



First IEEE/ACM/IFIP International Conference on Hardware/Software Codesign and System Synthesis
Marriott Hotel and Tennis Club Newport Beach, CA, October 1–3, 2003

Highlights include: Keynote by Irwin Mark Jacobs, Chairman of the Board and CEO, Qualcomm Inc.
Invited talks by Mojoy Chian, VP at MindSpeed Corp., and James Lin, VP at National Semiconductor Corp.
THREE excellent panels on system tools, systems research agenda, and future problems

The Conference will be awarding the following awards (sponsored by Synopsys):

Best Paper Award

Best Presentation Award

Each award carries a citation plus a cheque. The balloting for the awards will be done at the conference sessions and award announcements will be made at lunch on Friday, Oct 3, 2003. We sincerely look forward to your participation in the program and in selection of the award candidates.



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Day Zero: Tuesday, September 30, 2003

7:30a - 4:30p Southern California Embedded Systems Symposium, Beckman Center, UC Irvine
7:00p - 9:00p CODES+ISSS Registration and Reception Dinner at Marriott Hotel

Day One: Wednesday, October 1, 2003

8:00a - 9:00a Breakfast
9:00a - 9:15a Opening Welcome (Newport Ball Room)
9:15a - 10:30a Session 1 (Newport Ball Room) and (Catamaran / Trimaran / Brigantine)

1A Architectural Exploration and System Simulations

Chair: Walid Najjar, UC Riverside; Yukihiro Nakamura, Kyoto University

1. Virtual Synchronization Technique with OS Modeling for Fast and Time-accurate Cosimulation. *Youngmin Yi, Dohyung Kim, Soonhoi Ha (Seoul National Univ.)*
2. A Modular Simulation Framework for Architectural Exploration of On-Chip Interconnection Networks. *Tim Kogel, Malte Doerper, Andreas Wieferink, Rainer Leupers, Gerd Ascheid, Heinrich Meyr (Aachen University of Technology), Serge Goossens (CoWare)*
3. An Efficient Retargetable Framework for Instruction-Set Simulation. *Mehrdad Reshadi, Nikhil Bansal, Prabhat Mishra, Nikil Dutt (University of California, Irvine)*

1B Advances in System Modeling

Chair: Hiroto Yasuura, Kyushu University; Forrest Brewer, UC Santa Barbara

1. Invited Talk: Transaction Level Modeling. *Daniel Gajski, UC Irvine*
2. Extending the SystemC Synthesis Subset by Object Oriented Features. *Eike Grimpe, Frank Oppenheimer (OFFIS Research Institute)*
3. RTOS Scheduling in Transaction Level Model. *Haobo Yu, Andreas Gerstlauer, Daniel Gajski (University of California, Irvine)*

10:30a - 10:45a Break

10:45a - 12:00p Session 2 (Newport Ball Room) and (Catamaran / Trimaran / Brigantine)

2A Support for Real Time and OS Services in Embedded Systems

Chair: *Kwei-Jay Lin, UC Irvine; Petru Eles, Linköping University*

1. Generating Operating System Based Device Drivers for Peripheral Devices in Embedded Systems. *Shaojie Wang, Sharad Malik (Princeton University)*
2. Hardware Support for Real-time Operating Systems. *Paul Kohout (EVI Technology, LLC), Brinda Ganesh, Bruce L Jacob (University of Maryland, College Park)*
3. Invited Talk: Programming Embedded Networked Sensor Systems. *Feng Zhao*

2B Case studies in Embedded System

Chair: *Wayne Wolf, Princeton U.; Kazutoshi Wakabayashi, NEC Multimedia Research Lab*

1. Design Space Exploration of a HW-SW Co-designed GF(2^m) Galois Field Processor for FEC and Cryptography. *Wei Ming Lim and Mohammed Benaissa (University of Sheffield)*
2. A Fast Parallel -Solomon Decoder on a Reconfigurable Architecture. *Arezou Koochi, Nader Bagherzadeh, Chengzi Pan (University of California, Irvine)*
3. Analysis & Design of Architecture Systems for Speech Recognition on Modern Handheld-Computing Devices. *Andreas Hagen, Daniel A. Connors, Bryan L. Pellom (University of Colorado at Boulder)*

12:00p - 1:30p Lunch

1:30p - 2:30p Keynote Talk: (Newport Ball Room)

I1 Irwin Mark Jacobs, Chairman of the Board and CEO, Qualcomm Inc. "The Evolution of CDMA Wireless Devices Based on Advanced Chip Sets and BREW"

Chair: *Rajesh Gupta*

2:30p - 3:00p Break

3:00p - 4:30p Invited Sessions (Newport Ball Room) and (Catamaran / Trimaran / Brigantine)

A. Industry Best Practices and Upcoming Challenges in Embedded Software and Hardware

Chair: *Raul Camposano, Synopsys*

1. Mark Underseth, CEO of S2technologies, "Embedded Software Development for Wireless Handsets: Field Lessons in Extreme Programming"
2. Faraydon Karim, ST Fellow, ST Micro, "Parameteric Superscalar Microprocessors"

B. Challenges and New Directions in On-chip Communication

Chair: *Sharon Hu, U. Notre Dame; Jörg Henkel, NEC Lab*

1. Jason Cong, UCLA, "Architectural vs. Physical Solutions for On-Chip Communication Challenges"
2. Luca Carloni, UC Berkeley, "On-Chip Communication Design: Roadblocks and Avenues"
3. Douglas Burger, University of Texas at Austin, "Architecture and Synthesis for Multi-Cycle On-Chip Communication"

4:30p - 5:00p Break

5:00p - 6:30p Panel 1 (Newport Ball Room)

P1 System-level Design Tools: Who needs them, who has them and how much should they cost?

Moderator: *Grant Martin, Cadence Berkeley Labs*

Brian Bailey, Mentor Graphics; Pierre Paulin, ST Microelectronics; Pete Hardee, Coware; Roger Fordham, Motorola

Day Two: Thursday, October 2, 2003

7:30a - 8:30a Breakfast

8:30a - 9:30a Invited Talk: (Newport Ball Room)

I2 Mojoy Chian, VP of Core Technology, MindSpeed Corporation, "Economics of SOC Development: How can we make this a profitable endeavor?"

Chair: *Dan Gajski, UC Irvine*

9:30a - 9:45a Break

9:45a - 11:15a Panel 2 (Newport Ball Room)

P2 Driving Agenda in Systems Research

Organizer: *Nik Dutt, UC Irvine*

Janos Sztipanovits, Vanderbilt University Masaki Hirata, STARC Dan Radack, DARPA plus participant from EU

11:15a - 11:30a Break

11:30a - 12:20p Session 3 (Newport Ball Room) and (Catamaran / Trimaran / Brigantine)

3A System Modeling

Chair: Luciano Lavagno, Politecnico di Torino; Radu Marculescu, CMU

1. Design Optimization of Mixed Time/Event Triggered Distributed Embedded Systems. *Traian Pop, Petru Eles, Zebo Peng (Linköping University)*
2. Deriving Process Networks from Weakly Dynamic Applications in System-Level Design. *Todor Stefanov, Ed Depretere (Leiden Institute of Advanced Computer Science)*

3B: Case studies

Chair: Pierre Paulin, ST Micro; Majid Sarrafzadeh, UCLA

1. A Low-Cost and Low-Power Multi-Standard Video Encoder. *R. Peset Llopis, R. Sethuraman, C. Alba Pinto, H. Peters, S. Maul, M. Oosterhuis (Philips Research Laboratories)*
2. A Case Study of Mapping a Software-Defined Radio (SDR) application on a Reconfigurable DSP Core. *Behzad Mohebbi, Rafael Maestre, Eliseu Chavez Filho, Mark Davies (Morpho Technologies), Fadi Kurdahi (University of California, Irvine)*
3. A Codesigned On-Chip Logic Minimizer. *Roman Lysecky, Frank Vahid (Univ. of California, Riverside)*

12:20p - 1:45p Lunch

1:45p - 3:00p Session 4 (Newport Ball Room) and (Catamaran / Trimaran / Brigantine)

4A: Advances in Embedded Software Scheduling Techniques

Chair: Rolf Ernst, TU Braunschweig; Bob Walker, Kent State

1. On the Synthesis of Real-Time Embedded Software with Local and Global Deadlines. *Pao-Ann Hsiung and Cheng-Yi Lin (National Chung Cheng University)*
2. Pareto Optimization Based Run-time Task Scheduling for Embedded Systems. *Peng Yang and Francky Catthoor (IMEC)*
3. A Low Power Scheduler using Game Theory. *N. Ranganathan and Ashok K. Murugavel (University of South Florida)*

4B: Architectural Design for Embedded Systems

Chair: Alice Parker, USC; Faraydon Karim, ST Micro

1. VL-CDRAM: Variable Line Sized Cached DRAMs. *Ananth Hegde, Vijay Narayanan, Mahmut Kandemir, Mary Jane Irwin (Pennsylvania State University)*
2. A Low-cost Memory Architecture with NAND XIP (execute-in-place) for Mobile Embedded Systems. *Chanik Park, Jaeyu Seo, Sunghwan Bae, Hyojun Kim, Shinhan Kim (Samsung Electronics)*
3. Design Space Minimization with Timing and Code Size Optimization for Embedded DSP. *Qingfeng Zhuge, Zili Shao, Bin Xiao, Edwin H.-M. Sha (University of Texas at Dallas)*

3:00p - 3:30p Break

3:30p - 4:45p Session 5 (Newport Ball Room) and (Catamaran / Trimaran / Brigantine)

5A Work-in-progress session on innovative topics

Chair: Fadi Kurdahi, UC Irvine; Allen Wu, National Tsinghua Univ, Taiwan

1. SEAS: A System for Early Analysis of SoCs. *Reinaldo A. Bergamaschi*, Youngsoo Shin*, Nagu Dhanwada**, Subhrajit Bhattacharya*, William Dougherty**, Indira Nair*, John Darringer*, Sarala Paliwal** (*IBM T.J. Watson, **IBM EDA Lab)*
2. Programmer's Views of SoCs. *JoAnn M. Paul (Carnegie Mellon University)*
3. Security Wrappers and Power Analysis for SoC Technologies. *Cathy H. Gebotys, Y. Zhang (U. of Waterloo)*
4. First Results with eBlocks: Embedded Systems Building Blocks. *Susan Cotterell, Frank Vahid, Walid Najjar (University of California, Riverside)*

5B Verification and Modeling of Embedded Systems

Chair: Wolfgang Rosenstiel, TU Tuebingen; Harry Hsieh, UC Riverside

1. Verification of Design Decisions in ForSyDe. *Tarvo Raudvere, Ingo Sander, Ashish Kumar Singh and Axel Jantsch (Royal Institute of Technology)*
2. Optimization Model for Exploring Multiprocessor Mappings of Process Networks. *Cagkan Erbas (University of Amsterdam), Selin C. Erbas (Aachen Univ. of Technology), Andy D. Pimentel (Univ. of Amsterdam)*
3. A Fault Model Notation and Error-Control Scheme for Switch-to-Switch Buses in a Network-on-Chip. *Heiko Zimmer (Darmstadt University of Technology), Axel Jantsch (Royal Institute of Technology (KTH))*

5:00p - 7:45p Social Event

8:00p - 10:00p Banquet

Day Three: Friday, October 3, 2003

7:30a - 8:30a Breakfast

8:30a - 9:30a Invited Talk: (Newport Ball Room)

I3 James Lin, VP of Technology Infrastructure Group, National Semiconductor Corporation, "Design Technology Challenges for System and Chip Level Designs in Very Deep Submicron Technologies"

Chair: Don Thomas, CMU

9:30a - 9:45a Break

9:45a - 11:00a Session 6 (Newport Ball Room) and (Catamaran / Trimaran / Brigantine)

6A Performance Estimation in System Design

Chair: Mostapha Aboulhamid, Universite de Montreal; Raj Rajkumar, Carnegie Mellon Univ.

1. Schedule-Aware Performance Estimation of Communication Architecture for Efficient Design Space Exploration. *Sungchan Kim, Chaeseok Im, Soonhoi Ha (Seoul National University)*
2. Accurate Estimation of Cache-Related Preemption Delay. *Hemendra Singh Negi, Tulika Mitra, Abhik Roychoudhury (National University of Singapore)*
3. Early estimation of the size of VHDL projects. *W. Fornaciari, F. Salice, D.P. Scarpazza (Politecnico di Milano - DEI)*

6B Compiler Optimizations for Power, Performance

Chair: Miguel Miranda, IMEC; Margarida Jacome, UT Austin

1. Tracking Object Life Cycle for Leakage Energy Optimization. *G. Chen, N. Vijaykrishnan, M. Kandemir, Mary Jane Irwin (Pennsylvania State University), M. Wolczko (Sun Microsystems)*
2. Compiler Parallelization of C Programs for Multi-Core DSPs with Multiple Address Spaces. *Björn Franke, M. F. P. O'Boyle (University of Edinburgh)*
3. Architectural Analysis and Instruction-Set Optimization for Design of Network Protocol Processors. *Haiyong Xie, Li Zhao, Laxmi Bhuyan (University of California, Riverside)*

11:00a - 11:15a Break

11:15a - 12:45p Panel 3 (Newport Ball Room)

P3 The future of system-level design: can we find the right solution to the right problems at the right time?

Moderator: Reinaldo Bergamaschi, IBM Research

Panelists:

Wayne Wolf, Princeton University Rolf Ernst, TU Braunschweig Kees Vissers, UC Berkeley
 Jack Kouloheris, IBM Research Josh Fisher, Hewlett-Packard

12:45p - 1:00p Closing

1:00p - 2:30p Lunch and Announcement of **Best Paper and Best Presentation**

2:30p - EstiMedia Begins

For registration and travel information, or to register online, please see the conference web page
<http://www.ece.uci.edu/codes+iss/>