

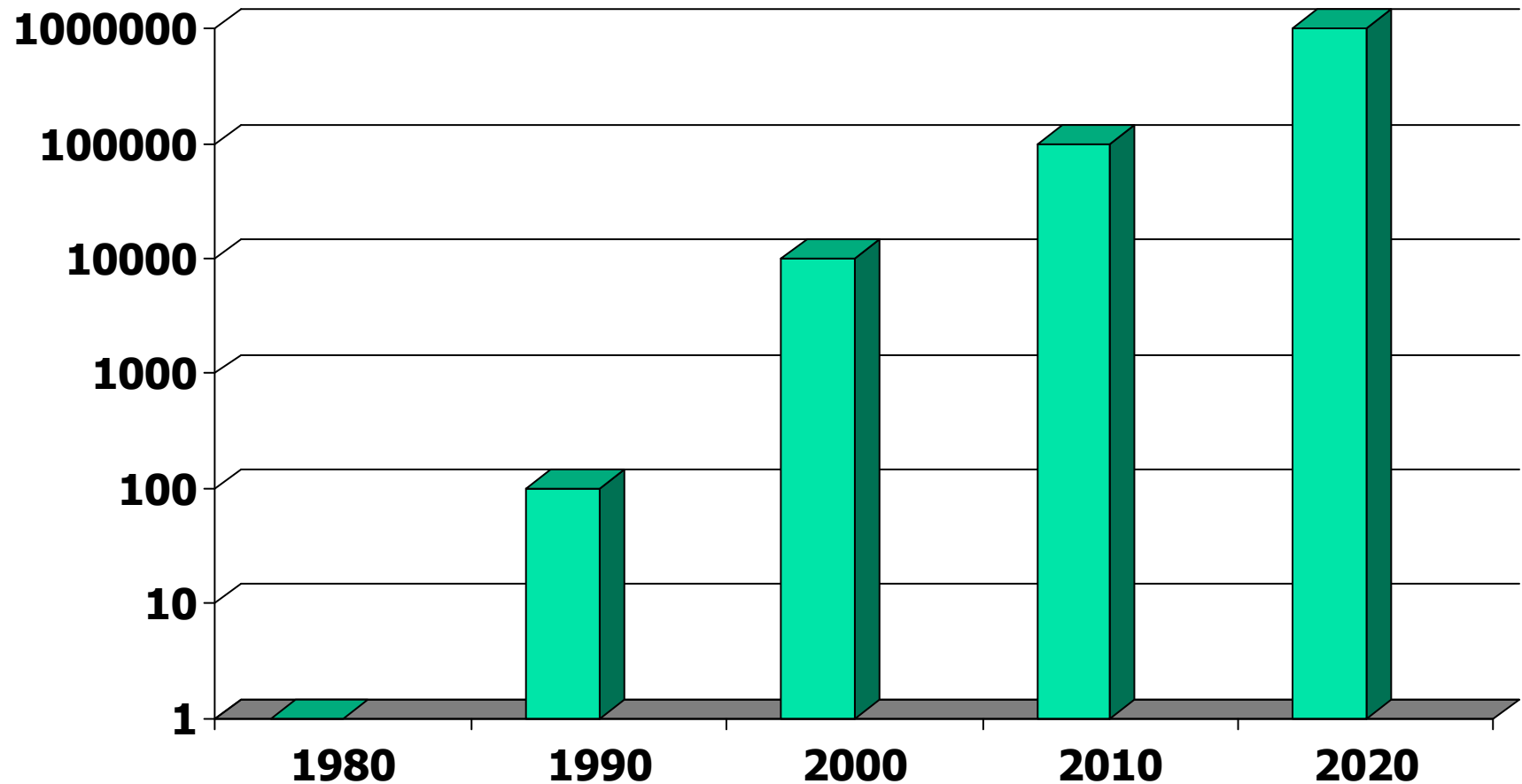
Platform Design and Platform Programming

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Platform design, platform programming





Platform design: No Asics anymore

- IBM, ST, Philips settop-box IC
 - Nvidia Graphics IC
 - Xilinx, Altera etc.
 - Qualcomm ICs
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- Development cost: \$10M – 100M
 - Only done for large markets
 - Mask Cost is NOT the biggest cost, engineering development cost is (verification!).



Platform programming

- Settop box: Vendor environment, Real-time OS
- Graphics: Microsoft DX10
- Xilinx, Altera: VHDL/verilog, Simulink

The real problem:

Route the data through the system, operand routing

Handle the concurrency

Use the dynamics of the application

Make sure it works!

NOT the problem: +, * , ALUs etc.



Your Thesis work:

- Correct programs
- Concurrent system programming above verilog/VHDL
- Architecture proposals that can stream data, without cache coherency (all virtual, on top of Xilinx, Altera!)
- Programming languages that are NOT control dominated, remove the for and if statements!
- Mapping these languages systematically onto architectures
- Garanteed Real-Time behavior
- Hardware thread scheduling
- Hide the 1000 cycle memory latency, systematic memory partitioning strategies.